PM-100
1983/1984

Unitrode POWER MOSFET

UNITRODE POWER MOSFET DATABOOK 1983/1984

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TABLE OF CONTENTS

PART NUMBER INDEX

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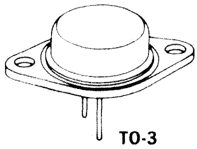
N-CHANNEL POWER MOSFETS

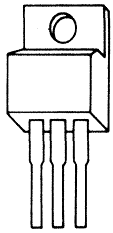


TO-3

V_{DS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	Part Numbers	I_D Continuous Drain Current (Amps)		I_{DM} Pulsed Drain Current (Amps)	$P_{D\ MAX}$ Power Dissipation (Watts)	Page
			100°C Case	25°C Case			
500	0.4	2N6770	7.75	12.0	48	150	41
500	0.4	UFN450	8.0	13.0	52	150	203
500	0.5	UFN452	7.0	12.0	48	150	203
500	0.85	UFN440	5.0	8.0	32	125	197
500	1.1	UFN442	4.0	7.0	28	125	197
500	1.5	2N6762	3.0	4.5	18	75	25
500	1.5	UFN430	3.0	4.5	18	75	191
500	2.0	UFN432	3.5	4.0	16	75	191
500	3.0	UFN420	1.5	2.5	10	40	185
500	4.0	UFN422	1.0	2.0	8	40	185
450	0.4	UFN451	8.0	13.0	52	150	203
450	0.5	2N6769	7.0	11.0	44	150	41
450	0.5	UFN453	7.0	12.0	48	150	203
450	0.85	UFN441	5.0	8.0	32	125	197
450	1.1	UFN443	4.0	7.0	28	125	197
450	1.5	UFN431	3.0	4.5	18	75	191
450	2.0	2N6761	2.5	4.0	16	75	25
450	2.0	UFN433	2.5	4.0	16	75	191
450	3.0	UFN421	1.5	2.5	10	40	185
450	4.0	UFN423	1.0	2.0	8	40	185
400	0.3	2N6768	9.0	14.0	56	150	37
400	0.3	UFN350	9.0	15.0	60	150	179
400	0.4	UFN352	8.0	13.0	52	150	179
400	0.55	UFN340	6.0	10.0	40	125	173
400	0.8	UFN342	5.0	8.0	32	125	173
400	1.0	2N6760	3.5	5.5	22	75	21
400	1.0	UFN330	3.5	5.5	22	75	167
400	1.5	UFN332	3.0	4.5	18	75	167
400	1.8	UFN320	2.0	3.0	12	40	161
400	2.5	UFN322	1.5	2.5	10	40	161
350	0.3	UFN351	9.0	15.0	60	150	179
350	0.4	2N6767	7.75	12.0	48	150	37
350	0.4	UFN353	8.0	13.0	52	150	179
350	0.55	UFN341	6.0	10.0	40	125	173
350	0.8	UFN343	5.0	8.0	32	125	173
350	1.0	UFN331	3.5	5.5	22	75	167
350	1.5	2N6759	3.0	4.5	18	75	21
350	1.5	UFN333	3.5	4.5	18	75	167
350	1.8	UFN321	2.0	3.0	12	40	161
350	2.5	UFN323	1.5	2.5	10	40	161

V_{DS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	Part Numbers	I_D Continuous Drain Current (Amps)		I_{DM} Pulsed Drain Current (Amps)	$P_{D\ MAX}$ Power Dissipation (Watts)	Page
			100°C Case	25°C Case			
200	0.085	2N6766	19.0	30.0	120	150	33
200	0.085	UFN250	19.0	30.0	120	150	155
200	0.12	UFN252	16.0	25.0	100	150	155
200	0.18	UFN240	11.0	18.0	72	125	149
200	0.22	UFN242	10.0	16.0	64	125	149
200	0.4	2N6758	6.0	9.0	36	75	17
200	0.4	UFN230	6.0	9.0	36	75	143
200	0.6	UFN232	5.0	8.0	32	75	143
200	0.8	UFN220	3.0	5.0	20	40	137
200	1.2	UFN222	2.5	4.0	16	40	137
150	0.085	UFN251	19.0	30.0	120	150	155
150	0.12	2N6765	16.0	25.0	100	150	33
150	0.12	UFN253	16.0	25.0	100	150	155
150	0.18	UFN241	11.0	18.0	72	125	149
150	0.22	UFN243	10.0	16.0	64	125	149
150	0.4	UFN231	6.0	9.0	36	75	143
150	0.6	2N6757	5.0	8.0	32	75	17
150	0.6	UFN233	5.0	8.0	32	75	143
150	0.8	UFN221	3.0	5.0	20	40	137
150	1.2	UFN223	2.5	4.0	16	40	137
100	0.055	2N6764	24.0	38.0	152	150	29
100	0.055	UFN150	25.0	40.0	160	150	131
100	0.08	UFN152	20.0	33.0	132	150	131
100	0.085	UFN140	17.0	27.0	108	125	125
100	0.11	UFN142	15.0	24.0	96	125	125
100	0.18	2N6756	9.0	14.0	56	75	13
100	0.18	UFN130	9.0	14.0	56	75	119
100	0.25	UIFN132	8.0	12.0	48	75	119
100	0.3	UFN120	5.0	8.0	32	40	113
100	0.4	UFN122	4.0	7.0	28	40	113
60	0.055	UFN151	25.0	40.0	160	150	131
60	0.08	2N6763	20.0	31.0	124	150	29
60	0.08	UFN153	20.0	33.0	132	150	131
60	0.085	UFN141	17.0	27.0	108	125	125
60	0.11	UFN143	15.0	24.0	96	125	125
60	0.18	UFN131	9.0	14.0	56	75	119
60	0.25	2N6755	8.0	12.0	48	75	13
60	0.25	UFN133	8.0	12.0	48	75	119
60	0.3	UFN121	5.0	8.0	32	40	113
60	0.4	UFN123	4.0	7.0	28	40	113

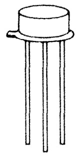
N-CHANNEL POWER MOSFETS



TO-220AB

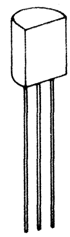
V_{DS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	Part Numbers	I_D Continuous Drain Current (Amps)		I_{DM} Pulsed Drain Current (Amps)	$P_{D\,MAX}$ Power Dissipation (Watts)	Page
			100°C Case	25°C Case			
500	0.85	UFN840	5.0	8.0	32	125	293
500	1.1	UFN842	4.0	7.0	28	125	293
500	1.5	UFN830	3.0	4.5	18	75	287
500	2.0	UFN832	2.5	4.0	16	75	287
500	3.0	UFN820	1.5	2.5	10	40	281
500	4.0	UFN822	1.0	2.0	8	40	281
450	0.85	UFN841	5.0	8.0	32	125	293
450	1.1	UFN843	4.0	7.0	28	125	293
450	1.5	UFN831	3.0	4.5	18	75	287
450	2.0	UFN833	2.5	4.0	16	75	287
450	3.0	UFN821	1.5	2.5	10	40	281
450	4.0	UFN823	1.0	2.0	8	40	281
400	0.55	UFN740	6.0	10.0	40	125	275
400	0.80	UFN742	5.0	8.0	32	125	275
400	1.0	UFN730	3.5	5.5	22	75	269
400	1.5	UFN732	3.0	4.5	18	75	269
400	1.8	UFN720	2.0	3.0	12	40	263
400	2.5	UFN722	1.5	2.5	10	40	263
400	3.6	UFN710	1.0	1.5	6	20	257
400	5.0	UFN712	0.8	1.3	5	20	257
350	0.55	UFN741	6.0	10.0	40	125	275
350	0.8	UFN743	5.0	8.0	32	125	275
350	1.0	UFN731	3.5	5.5	22	75	269
350	1.5	UFN733	3.0	4.5	18	75	269
350	1.8	UFN721	2.0	3.0	12	40	263
350	2.5	UFN723	1.5	2.5	10	40	263
350	3.6	UFN711	1.0	1.5	6	20	257
350	5.0	UFN713	0.8	1.3	5	20	257
200	0.18	UFN640	11.0	18.0	72	125	251
200	0.22	UFN642	10.0	16.0	64	125	251

V_{DS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	Part Numbers	I_D Continuous Drain Current (Amps)		I_{DM} Pulsed Drain Current (Amps)	$P_{D\,MAX}$ Power Dissipation (Watts)	Page
			100°C Case	25°C Case			
200	0.4	UFN630	6.0	9.0	36	75	245
200	0.6	UFN632	5.0	8.0	32	75	245
200	0.8	UFN620	3.0	5.0	20	40	239
200	1.2	UFN622	2.5	4.0	16	40	239
200	1.5	UFN610	1.5	2.5	10	20	233
200	2.4	UFN612	1.25	2.0	8	20	233
150	0.18	UFN641	11.0	18.0	72	125	251
150	0.22	UFN643	10.0	16.0	64	125	251
150	0.4	UFN631	6.0	9.0	36	75	245
150	0.6	UFN633	5.0	8.0	32	75	245
150	0.8	UFN621	3.0	5.0	20	40	239
150	1.2	UFN623	2.5	4.0	16	40	239
150	1.5	UFN611	1.5	2.5	10	20	223
150	2.4	UFN613	1.25	2.0	8	20	223
100	0.085	UFN540	17.0	27.0	108	125	227
100	0.11	UFN542	15.0	24.0	96	125	227
100	0.18	UFN530	9.0	14.0	56	75	221
100	0.25	UFN532	8.0	12.0	48	75	221
100	0.3	UFN520	5.0	8.0	32	40	215
100	0.4	UFN522	4.0	7.0	28	40	215
100	0.6	UFN510	2.5	4.0	16	20	209
100	0.8	UFN512	2.0	3.5	14	20	209
60	0.085	UFN541	17.0	27.0	108	125	227
60	0.11	UFN543	15.0	24.0	96	125	227
60	0.18	UFN531	9.0	14.0	56	75	221
60	0.25	UFN533	8.0	12.0	48	75	221
60	0.3	UFN521	5.0	8.0	32	40	215
60	0.4	UFN523	4.0	7.0	28	40	215
60	0.6	UFN511	2.5	4.0	16	20	209
60	0.8	UFN513	2.0	3.5	14	20	209



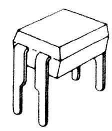
TO-39

V_{DS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	Part Numbers	I_D Continuous Drain Current (Amps) 100°C Case	I_D Continuous Drain Current (Amps) 25°C Case	I_{DM} Pulsed Drain Current (Amps)	$P_{D\,MAX}$ Power Dissipation (Watts)	Page
500	1.5	UFNF430	1.75	2.75	11	25	107
500	2.0	UFNF432	1.5	2.25	9	25	107
450	1.5	UFNF431	1.75	2.75	11	25	107
450	2.0	UFNF433	1.5	2.25	9	25	107
200	0.4	UFNF230	3.5	5.5	22	25	101
200	0.6	UFNF232	2.8	4.5	18	25	101
200	0.8	UFNF220	2.1	3.5	14	20	95
200	1.2	UFNF222	1.75	3.0	12	20	95
200	1.5	UFNF210	1.4	2.2	9	15	89
200	2.4	UFNF212	1.1	1.8	7.5	15	89
150	0.4	UFNF231	3.5	5.5	22	25	101
150	0.6	UFNF233	2.8	4.5	18	25	101
150	0.8	UFNF221	2.1	3.5	14	20	95
150	1.2	UFNF223	1.75	3.0	12	20	95
150	1.5	UFNF211	1.4	2.2	9	15	89
150	2.4	UFNF213	1.1	1.8	7.5	15	89
100	0.18	UFNF130	5.0	8.0	32	25	83
100	0.25	UFNF132	4.5	7.0	28	25	83
100	0.3	UFNF120	3.5	6.0	24	20	77
100	0.4	UFNF122	3.0	5.0	20	20	77
100	0.6	UFNF110	2.25	3.5	14	15	71
100	0.8	UFNF112	2.0	3.0	12	15	71
60	0.18	UFNF131	5.0	8.0	32	25	83
60	0.25	UFNF133	4.5	7.0	28	25	83
60	0.3	UFNF121	3.5	6.0	24	20	77
60	0.4	UFNF123	3.0	5.0	20	20	77
60	0.6	UFNF111	2.25	3.5	14	15	71
60	0.8	UFNF113	2.0	3.0	12	15	71



TO-92

V_{DS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	Part Numbers	I_D Continuous Drain Current (Amps) 25°C Case	I_{DM} Pulsed Drain Current (Amps)	$P_{D\,MAX}$ Power Dissipation (Watts)	Page
100	1.5	UFNA12	1.0	2.0	2.4	45
60	1.5	UFNA11	1.0	2.0	2.4	45



DIL-4

V_{DS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	Part Numbers	I_D Continuous Drain Current (Amps) 25°C Case	I_{DM} Pulsed Drain Current (Amps)	$P_{D\,MAX}$ Power Dissipation (Watts)	Page
200	1.5	UFND210	0.6	2.5	1.0	65
150	2.4	UFND213	0.45	1.8	1.0	65
100	0.3	UFND120	1.3	5.2	1.0	59
100	0.6	UFND110	1.0	4.0	1.0	53
100	0.8	UFND112	0.8	3.0	1.0	53
100	2.4	UFND1Z0	0.5	2.0	1.0	47
100	3.2	UFND1Z2	0.4	1.5	1.0	47
60	0.4	UFND123	1.1	4.4	1.0	59
60	0.6	UFND111	1.0	4.0	1.0	53
60	0.8	UFND113	0.8	3.0	1.0	53
60	2.4	UFND1Z1	0.5	2.0	1.0	47
60	3.2	UFND1Z3	0.4	1.5	1.0	47

POWER MOSFET TRANSISTORS

2N6755
2N6756

100 Volt, 0.18 Ohm
N-Channel

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

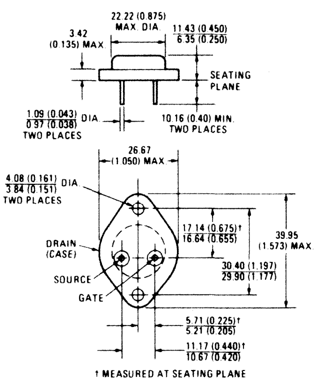
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6755	60V	0.25Ω	12A
2N6756	100V	0.18Ω	14A

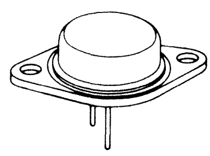
MECHANICAL SPECIFICATIONS

2N6755 2N6756



Dimensions in Millimeters and (Inches)

TO-3



UNITRODE

ABSOLUTE MAXIMUM RATINGS

Parameter		2N6755	2N6756	Units
V_{DS}	Drain – Source Voltage	60*	100*	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 1 MΩ)	60*	100*	V
I_D @ T_C = 25°C	Continuous Drain Current	12*	14*	A
I_D @ T_C = 100°C	Continuous Drain Current	8.0*	9.0*	A
I_{DM}	Pulsed Drain Current	25	30	A
V_{GS}	Gate – Source Voltage	±20*		V
P_D @ T_C = 25°C	Max. Power Dissipation	75* (See Fig. 11)		W
P_D @ T_C = 100°C	Max. Power Dissipation	30* (See Fig. 11)		W
	Linear Derating Factor	0.6* (See Fig. 11)		W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 µH 25	30	A
T_J T_{stg}	Operating and Storage Temperature Range	-55* to 150*		°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C

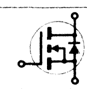
ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6755	60	–	–	V	V_{GS} = 0
		2N6756	100	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage (1)	2N6755	–	–	3.0*	V	V_{GS} = 10V, I_D = 12A
		2N6756	–	–	2.52*	V	V_{GS} = 10V, I_D = 14A
$R_{DS(on)}$	Static Drain-Source On-State Resistance (1)	2N6755	–	0.20	0.25*	Ω	V_{GS} = 10V, I_D = 8A
		2N6756	–	0.14	0.18*	Ω	V_{GS} = 10V, I_D = 9A
$R_{DS(on)}$	Static Drain-Source On-State Resistance (1)	2N6755	–	–	0.45*	Ω	V_{GS} = 10V, I_D = 8A, T_C = 125°C
		2N6756	–	–	0.33*	Ω	V_{GS} = 10V, I_D = 9A, T_C = 125°C
g_{fs}	Forward Transconductance (1)	ALL	4.0*	5.5	12.0*	S (℧)	V_{DS} = 15V, I_D = 9A
C_{iss}	Input Capacitance	ALL	350*	600	800*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	ALL	150*	300	500*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	ALL	50*	100	150*	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30*	ns	V_{DD} = 36V, I_D = 9A, Z_o = 15Ω
t_r	Rise Time	ALL	–	–	75*	ns	(See Figs. 13 and 14)
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	40*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	45*	ns	independent of operating temperature.)

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	1.67*	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

BODY-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	2N6755	–	–	12*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		2N6756	–	–	14*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6755	–	–	25	A	
		2N6756	–	–	30		
V_{SD}	Diode Forward Voltage (1)	2N6755	0.85*	–	1.7*	V	T_C = 25°C, I_S = 12A, V_{GS} = 0
		2N6756	0.90*	–	1.8*	V	T_C = 25°C, I_S = 14A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	300	–	ns	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/µs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.0	–	µC	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/µs

*JEDEC registered values. (1) Pulse Test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%

Fig. 1 — Clamped Inductive Test Circuit

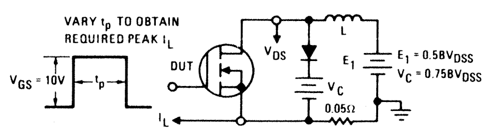


Fig. 2 — Clamped Inductive Waveforms

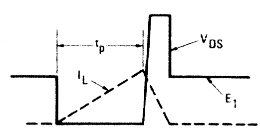


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Fig. 3 — Typical Output Characteristics

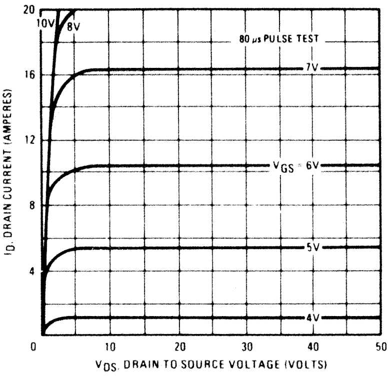


Fig. 4 — Typical Transfer Characteristics

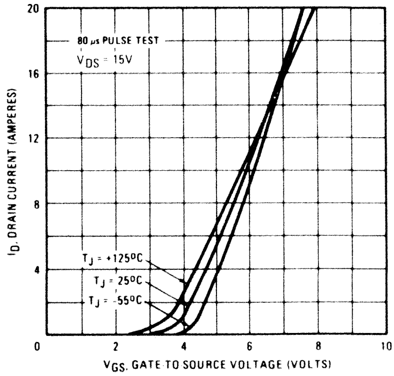


Fig. 5— Typical Saturation Characteristics (2N6755)

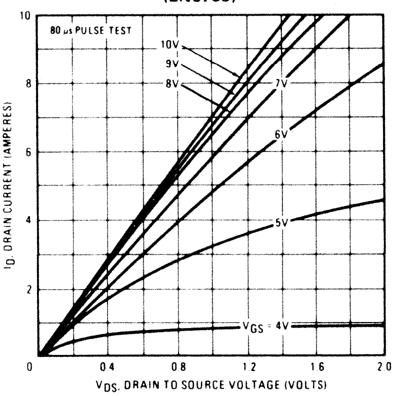


Fig. 6— Typical Saturation Characteristics (2N6756)

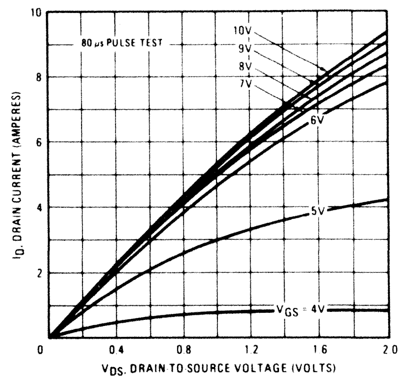


Fig. 7 — Typical Transconductance Vs. Drain Current

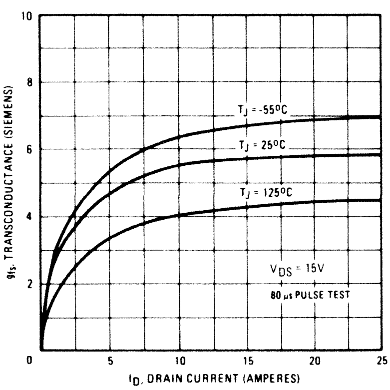


Fig. 8 — Maximum Safe Operating Area

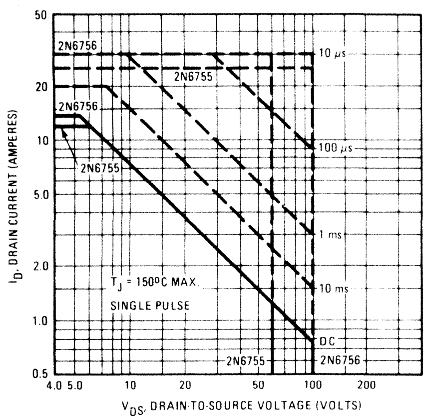


Fig. 9 — Normalized Typical On-Resistance Vs. Temperature

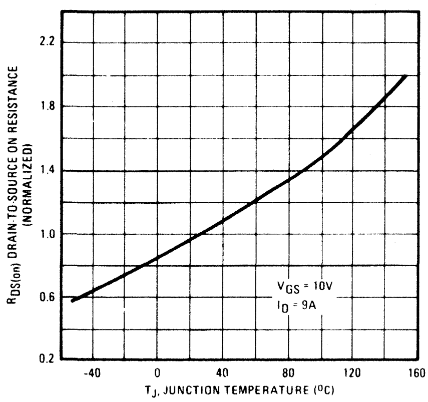


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

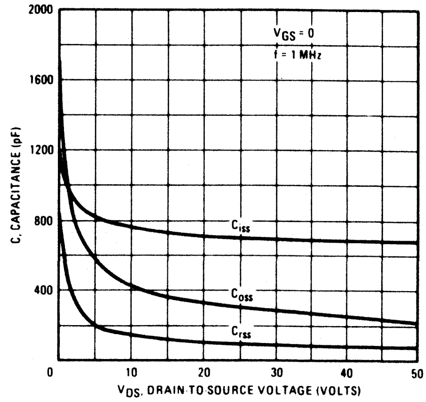


Fig. 11 — Power Vs. Temperature Derating Curve

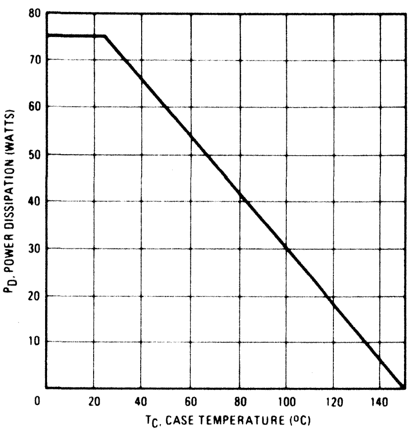


Fig. 12 — Typical Body-Drain Diode Forward Voltage

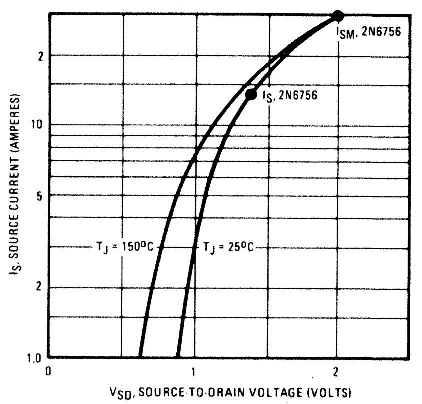


Fig. 13 — Switching Time Test Circuit

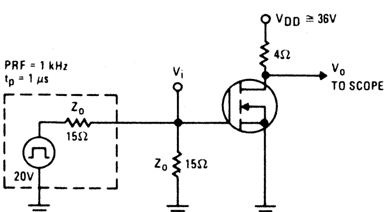
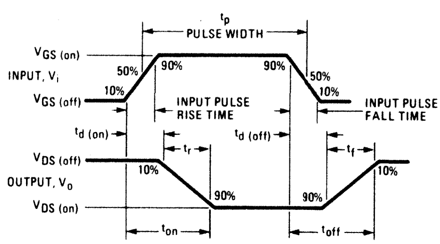


Fig. 14 — Switching Time Waveforms



POWER MOSFET TRANSISTORS

2N6757
2N6758

200 Volt, 0.4 Ohm
N-Channel

FEATURES
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

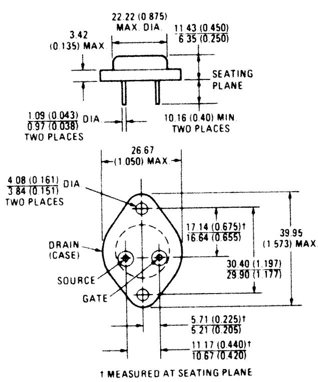
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6757	150V	0.6Ω	8A
2N6758	200V	0.4Ω	9A

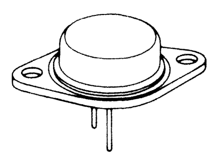
MECHANICAL SPECIFICATIONS

2N6757 2N6758



Dimensions in Millimeters and (Inches)

TO-3



UNITRODE

ABSOLUTE MAXIMUM RATINGS

Parameter		2N6757	2N6758	Units
V_{DS}	Drain – Source Voltage	150*	200*	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 1 MΩ)	150*	200*	V
I_D @ T_C = 25°C	Continuous Drain Current	8.0*	9.0*	A
I_D @ T_C = 100°C	Continuous Drain Current	5.0*	6.0*	A
I_{DM}	Pulsed Drain Current	12	15	A
V_{GS}	Gate – Source Voltage	±20*		V
P_D @ T_C = 25°C	Max. Power Dissipation	75* (See Fig. 11)		W
P_D @ T_C = 100°C	Max. Power Dissipation	30* (See Fig. 11)		W
	Linear Derating Factor	0.6* (See Fig. 11)		W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH 12	15	A
T_J T_{stg}	Operating and Storage Temperature Range	-55* to 150*		°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C

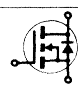
ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6757	150	–	–	V	V_{GS} = 0
		2N6758	200	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6757	–	–	4.8*	V	V_{GS} = 10V, I_D = 8A
		2N6758	–	–	3.6*	V	V_{GS} = 10V, I_D = 9A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6757	–	0.4	0.6*	Ω	V_{GS} = 10V, I_D = 5A
		2N6758	–	0.25	0.4*	Ω	V_{GS} = 10V, I_D = 6A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6757	–	–	1.13*	Ω	V_{GS} = 10V, I_D = 5A, T_C = 125°C
		2N6758	–	–	0.75*	Ω	V_{GS} = 10V, I_D = 6A, T_C = 125°C
g_{fs}	Forward Transconductance ①	ALL	3.0*	5.0	9.0*	S (℧)	V_{DS} = 15V, I_D = 6A
C_{iss}	Input Capacitance	ALL	350*	600	800*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	ALL	100*	250	450*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	ALL	40*	80	150*	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	–	–	30*	ns	V_{DD} ≅ 90V, I_D = 6A, Z_o = 15Ω
t_r	Rise Time	ALL	–	–	50*	ns	(See Figs. 13 and 14)
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	–	–	50*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	40*	ns	independent of operating temperature.)

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	1.67*	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

BODY-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	2N6757	–	–	8.0*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		2N6758	–	–	9.0*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6757	–	–	12	A	
		2N6758	–	–	15		
V_{SD}	Diode Forward Voltage ①	2N6757	0.75*	–	1.50*	V	T_C = 25°C, I_S = 8A, V_{GS} = 0
		2N6758	0.80*	–	1.60*	V	T_C = 25°C, I_S = 9A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	650	–	ns	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	10	–	μC	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

Fig. 1 — Clamped Inductive Test Circuit

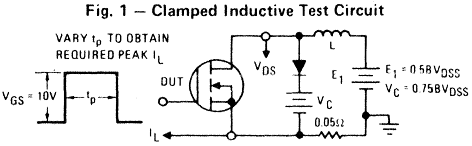


Fig. 2 — Clamped Inductive Waveforms

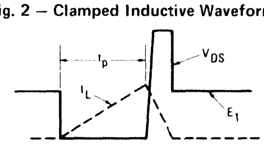


Fig. 3 — Typical Output Characteristics

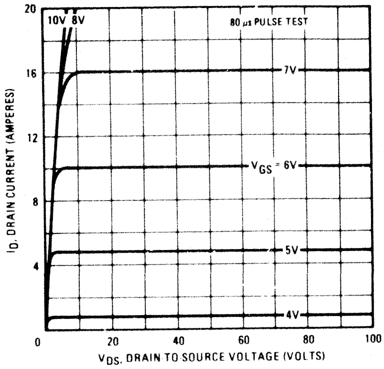


Fig. 4 — Typical Transfer Characteristics

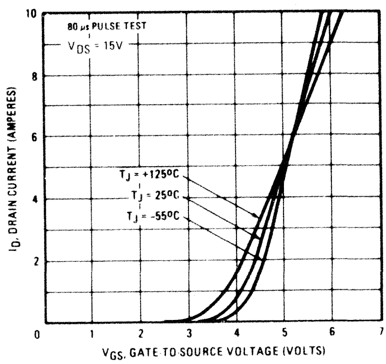


Fig. 5— Typical Saturation Characteristics (2N6757)

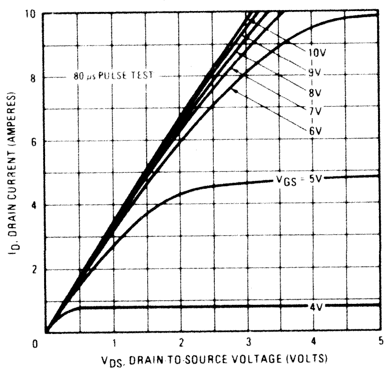


Fig. 6— Typical Saturation Characteristics (2N6758)

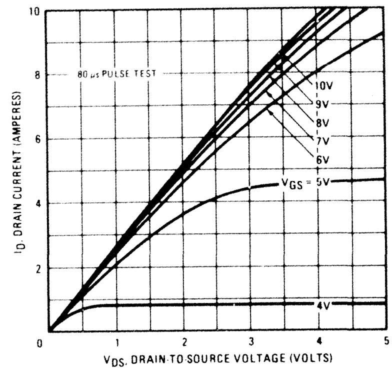


Fig. 7 — Typical Transconductance Vs. Drain Current

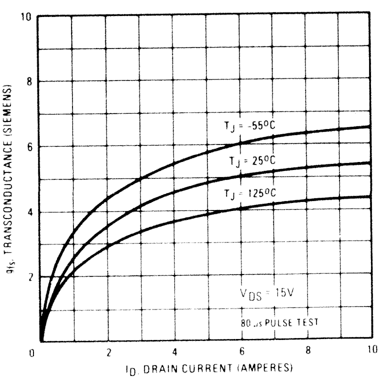


Fig. 8 — Maximum Safe Operating Area

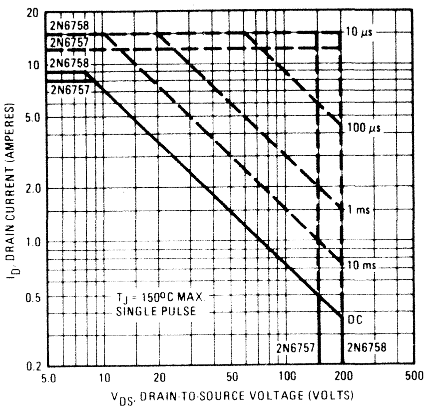


Fig. 9 — Normalized Typical On-Resistance Vs. Temperature

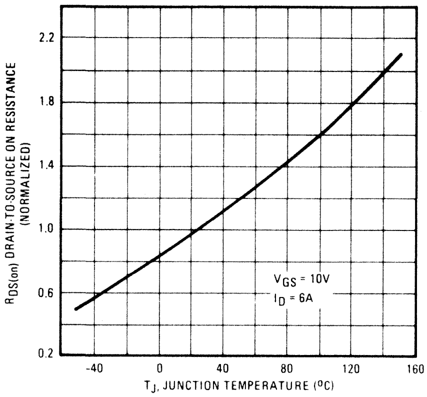


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

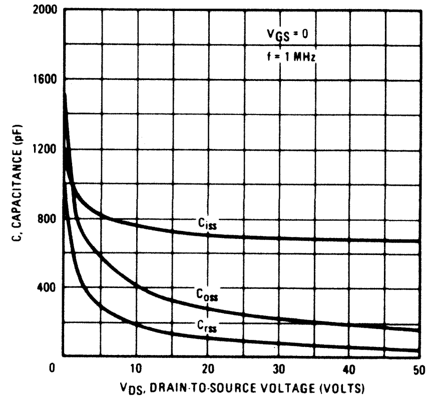


Fig. 11 — Power Vs. Temperature Derating Curve

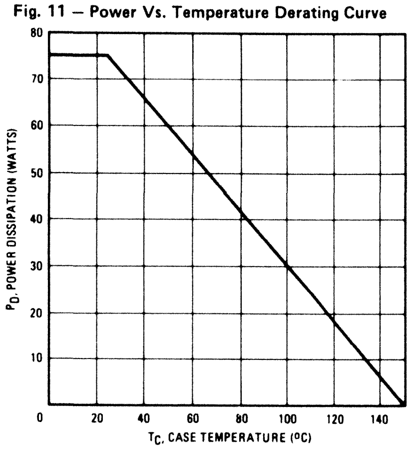


Fig. 12 — Typical Body-Drain Diode Forward Voltage

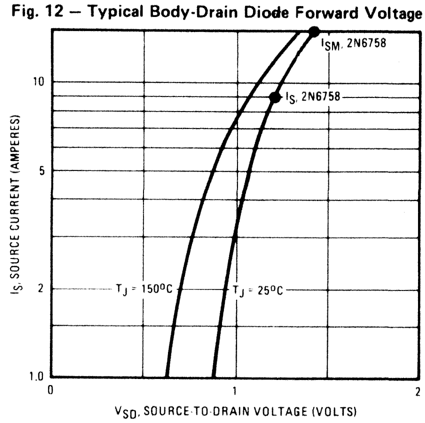


Fig. 13 — Switching Time Test Circuit

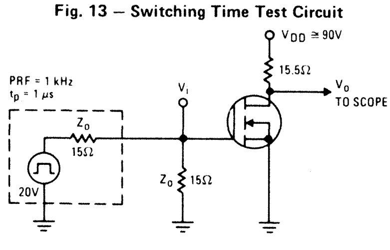
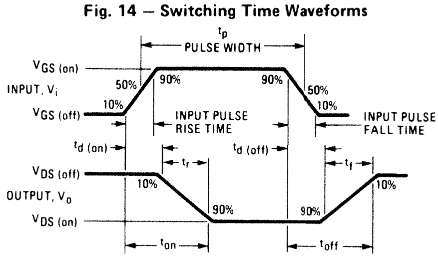


Fig. 14 — Switching Time Waveforms



POWER MOSFET TRANSISTORS

2N6759
2N6760

400 Volt, 1.0 Ohm
N-Channel

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

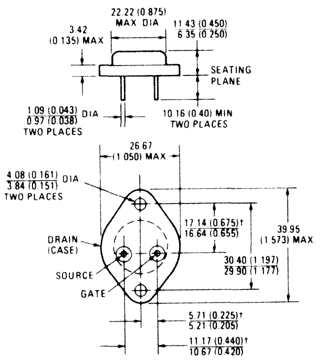
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6759	350V	1.5Ω	4.5A
2N6760	400V	1.0Ω	5.5A

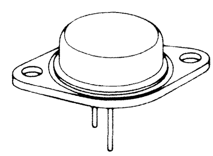
MECHANICAL SPECIFICATIONS

2N6759 2N6760



Dimensions in Millimeters and (Inches)

TO-3



ABSOLUTE MAXIMUM RATINGS

Parameter		2N6759	2N6760	Units
V_{DS}	Drain – Source Voltage	350*	400*	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 1 MΩ)	350*	400*	V
I_D @ T_C = 25°C	Continuous Drain Current	4.5*	5.5*	A
I_D @ T_C = 100°C	Continuous Drain Current	3.0*	3.5*	A
I_{DM}	Pulsed Drain Current	7.0	8.0	A
V_{GS}	Gate – Source Voltage	±20*		V
P_D @ T_C = 25°C	Max. Power Dissipation	75* (See Fig. 11)		W
P_D @ T_C = 100°C	Max. Power Dissipation	30* (See Fig. 11)		W
	Linear Derating Factor	0.6* (See Fig. 11)		W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH 7.0	8.0	A
T_J T_{stg}	Operating and Storage Temperature Range	-55* to 150*		°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6759	350	–	–	V	V_{GS} = 0
		2N6760	400	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage (1)	2N6759	–	–	7.0*	V	V_{GS} = 10V, I_D = 4.5A
		2N6760	–	–	6.7*	V	V_{GS} = 10V, I_D = 5.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance (1)	2N6759	–	1.0	1.5*	Ω	V_{GS} = 10V, I_D = 3A
		2N6760	–	0.8	1.0*	Ω	V_{GS} = 10V, I_D = 3.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance (1)	2N6759	–	–	3.3*	Ω	V_{GS} = 10V, I_D = 3A, T_C = 125°C
		2N6760	–	–	2.2*	Ω	V_{GS} = 10V, I_D = 3.5A, T_C = 125°C
g_{fs}	Forward Transconductance (1)	ALL	3.0*	4.5	9.0*	S (℧)	V_{DS} = 15V, I_D = 3.5A
C_{iss}	Input Capacitance	ALL	350*	600	800*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	50*	150	300*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	20*	40	80*	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30*	ns	V_{DD} ≧ 175V, I_D = 3.5A, Z_o = 15Ω
t_r	Rise Time	ALL	–	–	35*	ns	(See Figs. 13 and 14)
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	55*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	35*	ns	independent of operating temperature.)

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	1.67*	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

BODY-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	2N6759	–	–	4.5*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		2N6760	–	–	5.5*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6759	–	–	7.0	A	
		2N6760	–	–	8.0		
V_{SD}	Diode Forward Voltage (1)	2N6759	0.70*	–	1.4*	V	T_C = 25°C, I_S = 4.5A, V_{GS} = 0
		2N6760	0.75*	–	1.5*	V	T_C = 25°C, I_S = 5.5A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	550	–	ns	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	8.0	–	μC	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs

*JEDEC registered values. (1) Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

Fig. 1 – Clamped Inductive Test Circuit

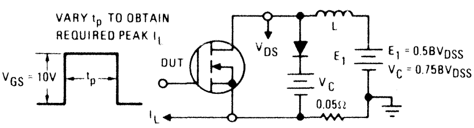


Fig. 2 – Clamped Inductive Waveforms

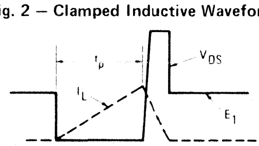


Fig. 3 – Typical Output Characteristics

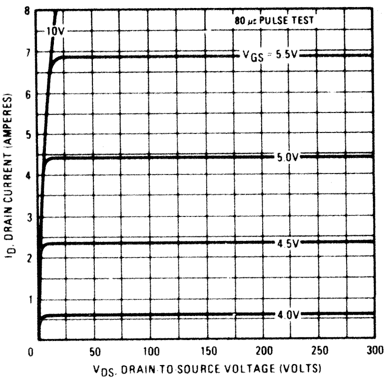


Fig. 4 – Typical Transfer Characteristics

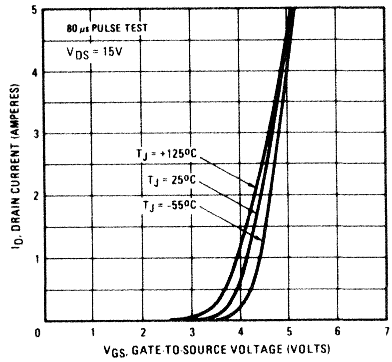


Fig. 5– Typical Saturation Characteristics (2N6759)

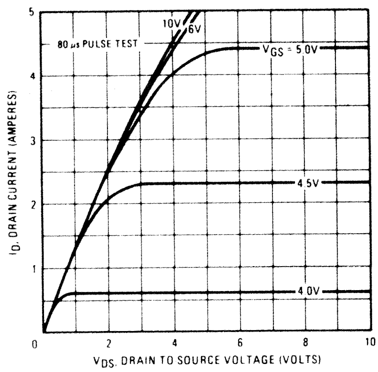


Fig. 6– Typical Saturation Characteristics (2N6760)

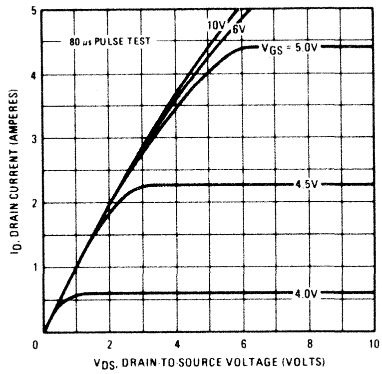


Fig. 7 – Typical Transconductance Vs. Drain Current

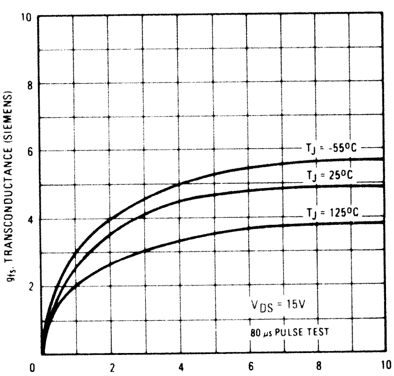


Fig. 8 – Maximum Safe Operating Area

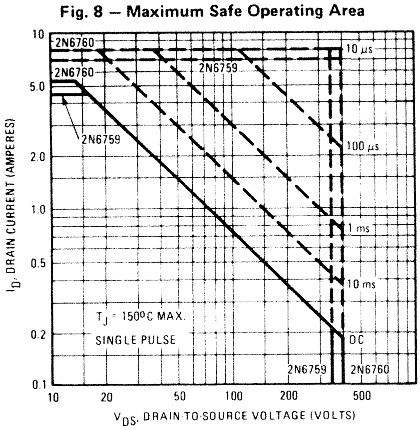


Fig. 9 — Normalized Typical On-Resistance Vs. Temperature

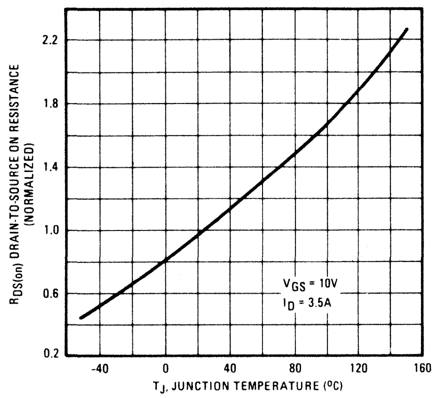


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

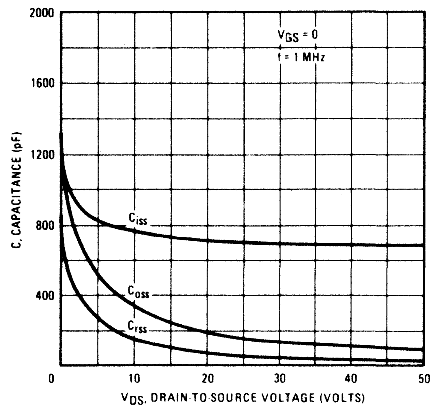


Fig. 11 — Power Vs. Temperature Derating Curve

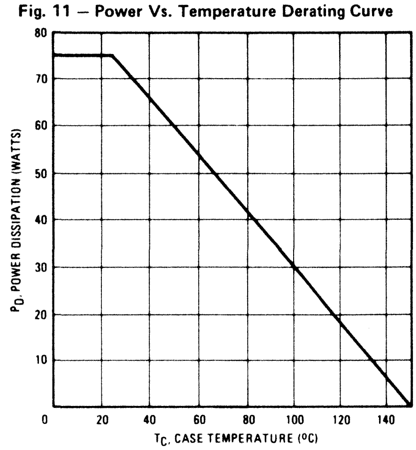


Fig. 12 — Typical Body-Drain Diode Forward Voltage

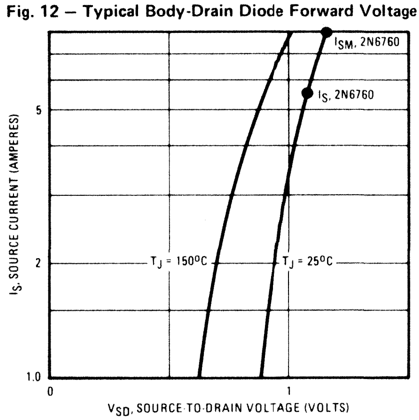


Fig. 13 — Switching Time Test Circuit

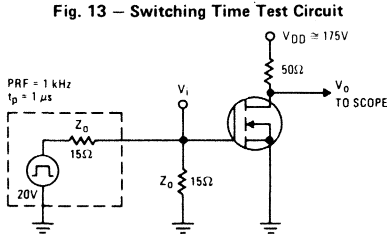
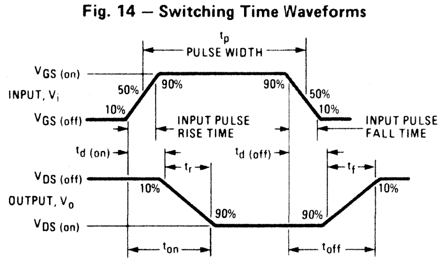


Fig. 14 — Switching Time Waveforms



POWER MOSFET TRANSISTORS

500 Volt, 1.5 Ohm
N-Channel

2N6761
2N6762

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

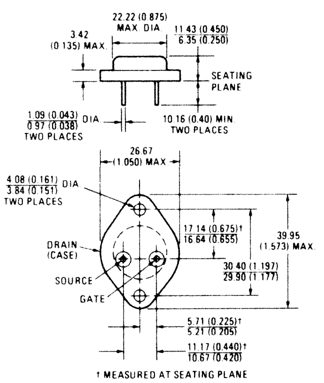
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6761	450V	2.0Ω	4.0A
2N6762	500V	1.5Ω	4.5A

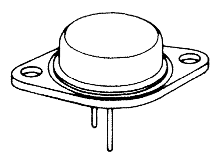
MECHANICAL SPECIFICATIONS

2N6761 2N6762



Dimensions in Millimeters and (Inches)

TO-3



UNITRODE

ABSOLUTE MAXIMUM RATINGS

Parameter		2N6761	2N6762	Units
V_{DS}	Drain – Source Voltage	450*	500*	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 1 MΩ)	450*	500*	V
I_D @ T_C = 25°C	Continuous Drain Current	4.0*	4.5*	A
I_D @ T_C = 100°C	Continuous Drain Current	2.5*	3.0*	A
I_{DM}	Pulsed Drain Current	6.0	7.0	A
V_{GS}	Gate – Source Voltage	±20*		V
P_D @ T_C = 25°C	Max. Power Dissipation	75* (See Fig. 11)		W
P_D @ T_C = 100°C	Max. Power Dissipation	30* (See Fig. 11)		W
	Linear Derating Factor	0.6* (See Fig. 11)		W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH 6.0	7.0	A
T_J T_{stg}	Operating and Storage Temperature Range	-55* to 150*		°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C

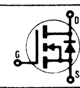
ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6761	450	–	–	V	V_{GS} = 0
		2N6762	500	–	–	V	I_D = 4.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = 0.8 x Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 25°C to 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage (1)	2N6761	–	–	8.0*	V	V_{GS} = 10V, I_D = 4A
		2N6762	–	–	7.7*	V	V_{GS} = 10V, I_D = 4.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance (1)	2N6761	–	1.5	2.0*	Ω	V_{GS} = 10V, I_D = 2.5A
		2N6762	–	1.3	1.5*	Ω	V_{GS} = 10V, I_D = 3.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance (1)	2N6761	–	–	4.4*	Ω	V_{GS} = 10V, I_D = 2.5A, T_C = 125°C
		2N6762	–	–	3.3*	Ω	V_{GS} = 10V, I_D = 3.0A, T_C = 125°C
g_{fs}	Forward Transconductance (1)	ALL	2.5*	3.5	7.5*	S (℧)	V_{DS} = 16V, I_D = 3A
C_{iss}	Input Capacitance	ALL	350*	600	800*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	ALL	25*	100	200*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	ALL	15*	30	60*	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30*	ns	V_{DD} ≅ 225V, I_D = 3A, Z_o = 15Ω
t_r	Rise Time	ALL	–	–	30*	ns	(See Figs. 13 and 14)
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	55*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	30*	ns	independent of operating temperature.)

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	1.67*	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

BODY-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	2N6761	–	–	4.0*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		2N6762	–	–	4.5*	A	
I_{SM}	Pulsed Source Current (Body Diode)	2N6761	–	–	6.0	A	
		2N6762	–	–	7.0	A	
V_{SD}	Diode Forward Voltage (1)	2N6761	0.65*	–	1.3*	V	T_C = 25°C, I_S = 4A, V_{GS} = 0
		2N6762	0.7*	–	1.4*	V	T_C = 25°C, I_S = 4.5A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	500	–	ns	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	7.0	–	μC	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs

*JEDEC registered values. (1) Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

Fig. 1 — Clamped Inductive Test Circuit

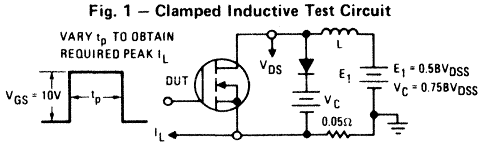


Fig. 2 — Clamped Inductive Waveforms

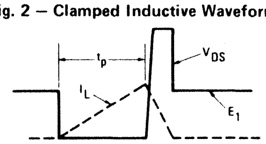


Fig. 3 — Typical Output Characteristics

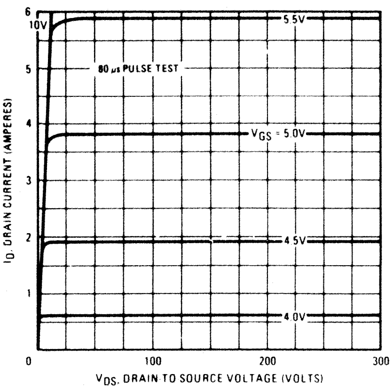


Fig. 4 — Typical Transfer Characteristics

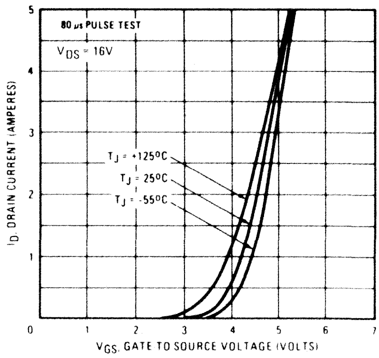


Fig. 5— Typical Saturation Characteristics (2N6761)

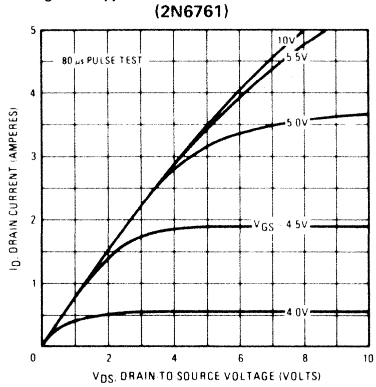


Fig. 6— Typical Saturation Characteristics (2N6762)

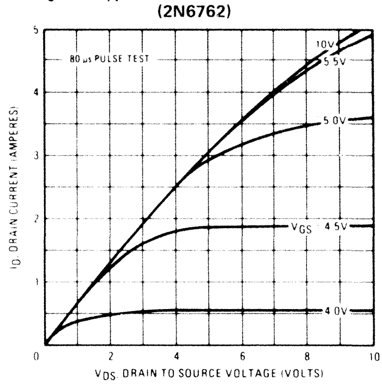


Fig. 7 — Typical Transconductance Vs. Drain Current

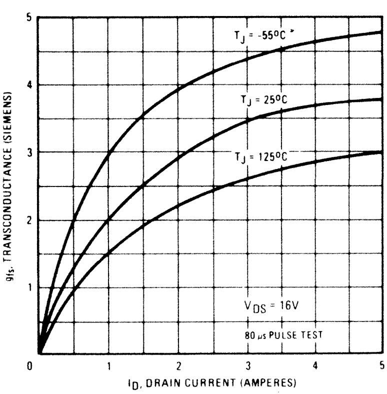


Fig. 8 — Maximum Safe Operating Area

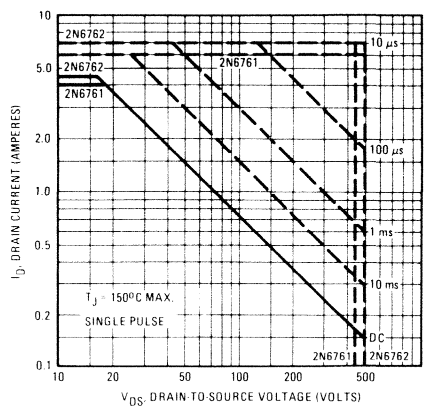


Fig. 9 — Normalized Typical On-Resistance Vs. Temperature

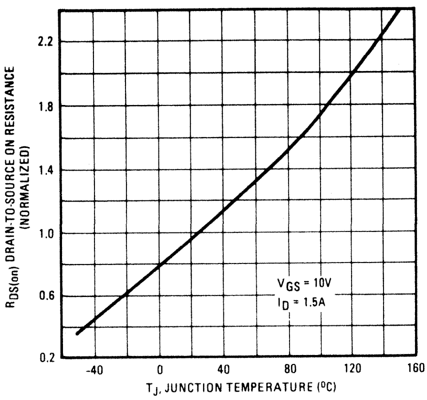


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

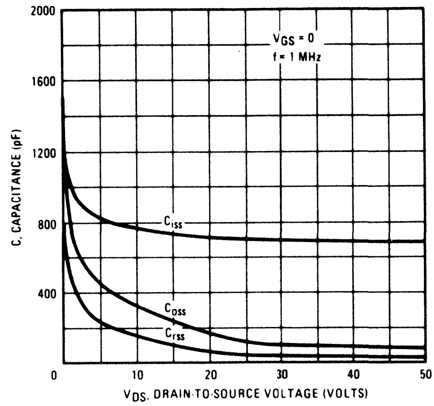


Fig. 11 — Power Vs. Temperature Derating Curve

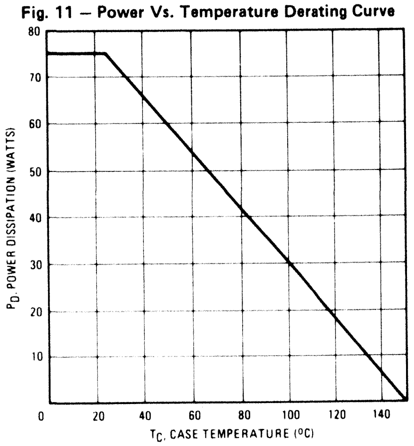


Fig. 12 — Typical Body-Drain Diode Forward Voltage

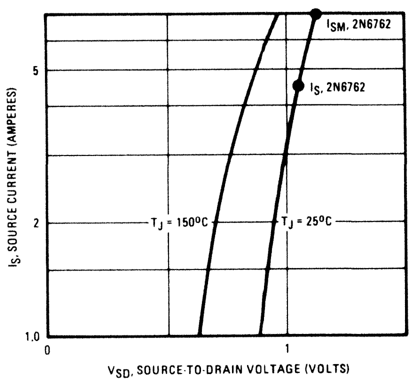


Fig. 13 — Switching Time Test Circuit

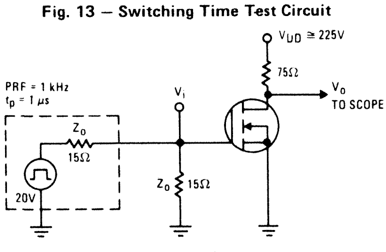
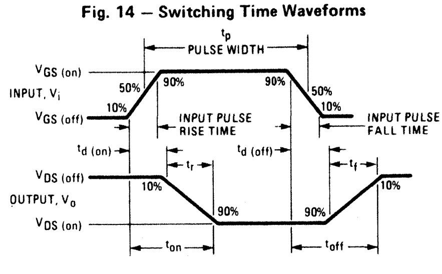


Fig. 14 — Switching Time Waveforms



POWER MOSFET TRANSISTORS

100 Volt, 0.055 Ohm
N-Channel

2N6763
2N6764

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

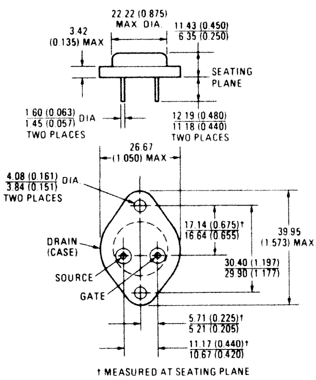
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6763	60V	0.08Ω	31A
2N6764	100V	0.055Ω	38A

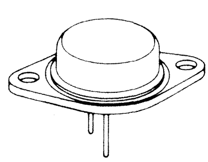
MECHANICAL SPECIFICATIONS

2N6763 2N6764



Dimensions in Millimeters and (Inches)

TO-3 (Modified)



UNITRODE

ABSOLUTE MAXIMUM RATINGS

Parameter		2N6763	2N6764	Units
V_{DS}	Drain – Source Voltage	60*	100*	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 1 MΩ)	60*	100*	V
I_D @ T_C = 25°C	Continuous Drain Current	31*	38*	A
I_D @ T_C = 100°C	Continuous Drain Current	20*	24*	A
I_{DM}	Pulsed Drain Current	60	70	A
V_{GS}	Gate – Source Voltage	±20*		V
P_D @ T_C = 25°C	Max. Power Dissipation	150* (See Fig. 11)		W
P_D @ T_C = 100°C	Max. Power Dissipation	60* (See Fig. 11)		W
	Linear Derating Factor	1.2* (See Fig. 11)		W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH 60	70	A
T_J T_{stg}	Operating and Storage Temperature Range	-55* to 150*		°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C

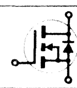
ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6763	60	–	–	V	V_{GS} = 0
		2N6764	100	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage (1)	2N6763		–	2.48*	V	V_{GS} = 10V I_D = 31A
		2N6764	–		2.09*	V	V_{GS} = 10V, I_D = 38A
$R_{DS(on)}$	Static Drain-Source On-State Resistance (1)	2N6763	–	0.06	0.08*	Ω	V_{GS} = 10V, I_D = 20A
		2N6764	–	0.045	0.055*	Ω	V_{GS} = 10V, I_D = 24A
$R_{DS(on)}$	Static Drain-Source On-State Resistance (1)	2N6763	–	–	0.136*	Ω	V_{GS} = 10V, I_D = 20A, T_C = 125°C
		2N6764	–	–	0.094*	Ω	V_{GS} = 10V, I_D = 24A, T_C = 125°C
g_{fs}	Forward Transconductance (1)	ALL	9.0*	12.5	27*	S (℧)	V_{DS} = 15V, I_D = 24A
C_{iss}	Input Capacitance	ALL	1000*	2000	3000*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	ALL	500*	1000	1500*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	ALL	150*	350	500*	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	–	–	35*	ns	V_{DD} ≅ 24V, I_D = 24A, Z_o = 4.7Ω
t_r	Rise Time	ALL	–	–	100*	ns	(See Figs. 13 and 14)
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	–	–	125*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	100*	ns	independent of operating temperature.)

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	0.83*	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

BODY-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	2N6763	–	–	31*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		2N6764	–	–	38*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6763	–	–	60	A	
		2N6764	–	–	70		
V_{SD}	Diode Forward Voltage (1)	2N6763	0.90*	–	1.8*	V	T_C = 25°C, I_S = 31A, V_{GS} = 0
		2N6764	0.95*	–	1.9*	V	T_C = 25°C, I_S = 38A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	500	–	ns	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	10	–	μC	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs

*JEDEC registered values. (1) Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

Fig. 1 — Clamped Inductive Test Circuit

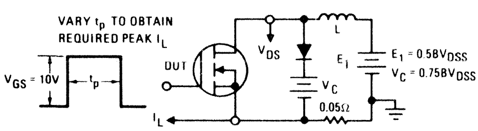


Fig. 2 — Clamped Inductive Waveforms

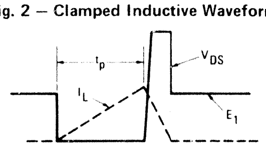


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Fig. 3 — Typical Output Characteristics

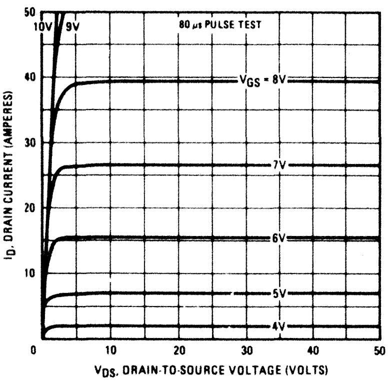


Fig. 4 — Typical Transfer Characteristics

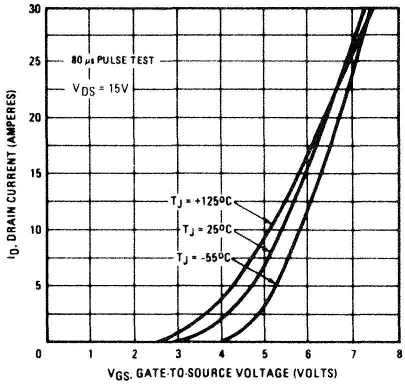


Fig. 5— Typical Saturation Characteristics (2N6763)

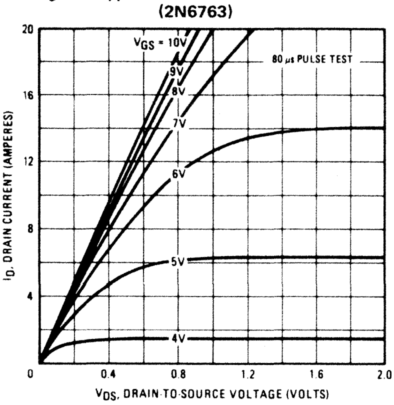


Fig. 6— Typical Saturation Characteristics (2N6764)

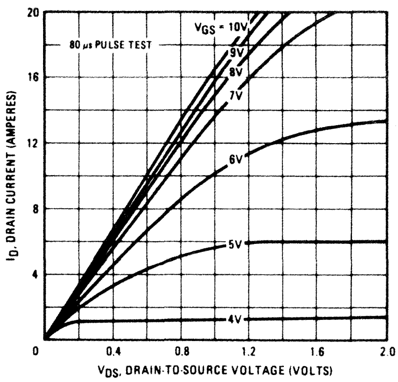


Fig. 7 — Typical Transconductance Vs. Drain Current

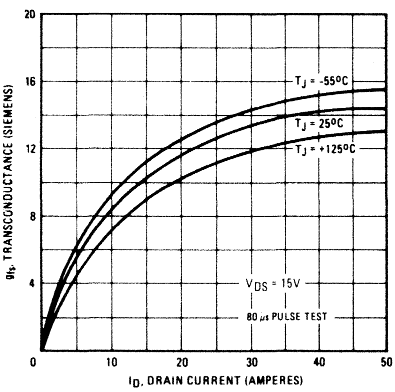


Fig. 8 — Maximum Safe Operating Area

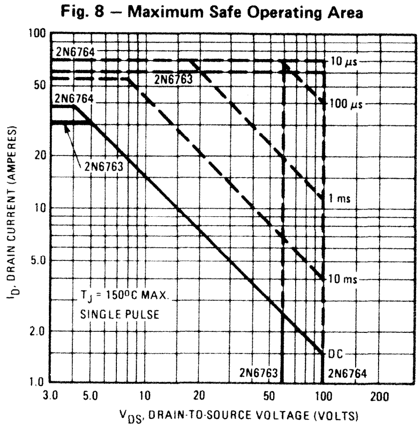


Fig. 9 — Normalized Typical On-Resistance Vs. Temperature

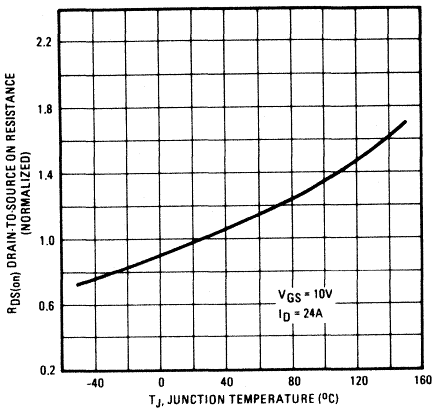


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

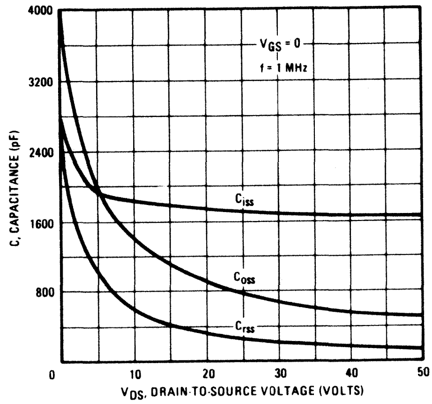


Fig. 11 — Power Vs. Temperature Derating Curve

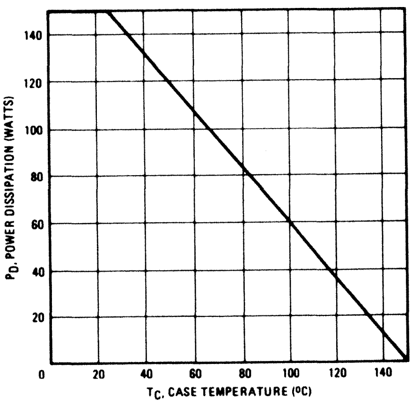


Fig. 12 — Typical Body-Drain Diode Forward Voltage

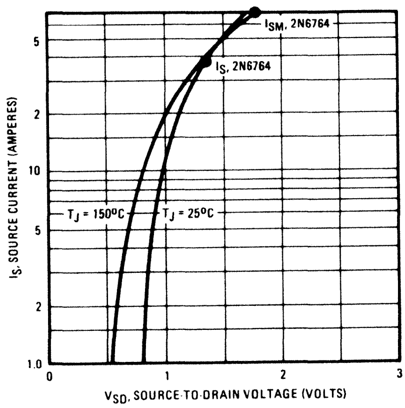


Fig. 13 — Switching Time Test Circuit

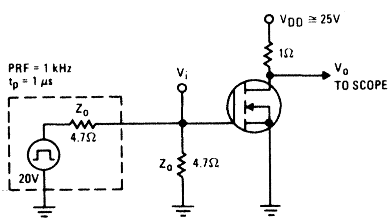
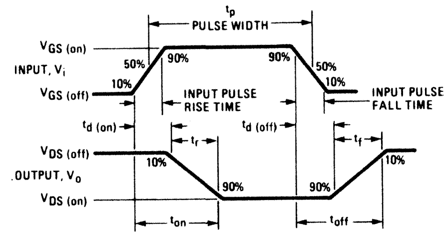


Fig. 14 — Switching Time Waveforms



POWER MOSFET TRANSISTORS

2N6765
2N6766

200 Volt, 0.085 Ohm
N-Channel

FEATURES
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

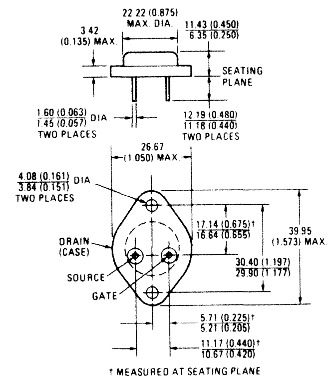
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6765	150V	0.120Ω	25A
2N6766	200V	0.085Ω	30A

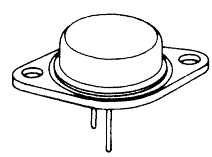
MECHANICAL SPECIFICATIONS

2N6765 2N6766



Dimensions in Millimeters and (Inches)

TO-3 (Modified)



UNITRODE

4/83

ABSOLUTE MAXIMUM RATINGS

Parameter		2N6765	2N6766	Units
V_{DS}	Drain – Source Voltage	150*	200*	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 1 MΩ)	150*	200*	V
I_D @ T_C = 25°C	Continuous Drain Current	25*	30*	A
I_D @ T_C = 100°C	Continuous Drain Current	16*	19*	A
I_{DM}	Pulsed Drain Current	50	60	A
V_{GS}	Gate – Source Voltage	±20*		V
P_D @ T_C = 25°C	Max. Power Dissipation	150* (See Fig. 11)		W
P_D @ T_C = 100°C	Max. Power Dissipation	60* (See Fig. 11)		W
	Linear Derating Factor	1.2* (See Fig. 11)		W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH 50	60	A
T_J T_{stg}	Operating and Storage Temperature Range	-55* to 150*		°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6765	150	–	–	V	V_{GS} = 0
		2N6766	200	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage (1)	2N6765	–	–	3.0*	V	V_{GS} = 10V, I_D = 25A
		2N6766	–	–	2.7*	V	V_{GS} = 10V, I_D = 30A
$R_{DS(on)}$	Static Drain-Source On-State Resistance (1)	2N6765	–	0.09	0.12*	Ω	V_{GS} = 10V, I_D = 16A
		2N6766	–	0.07	0.085*	Ω	V_{GS} = 10V, I_D = 19A
$R_{DS(on)}$	Static Drain-Source On-State Resistance (1)	2N6765	–	–	0.216*	Ω	V_{GS} = 10V, I_D = 16A, T_C = 125°C
		2N6766	–	–	0.153*	Ω	V_{GS} = 10V, I_D = 19A, T_C = 125°C
g_{fs}	Forward Transconductance (1)	ALL	9.0*	15.5	27*	S (℧)	V_{DS} = 15V, I_D = 19A
C_{iss}	Input Capacitance	ALL	1000*	2000	3000*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	ALL	450*	800	1200*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	ALL	150*	300	500*	pF	
$t_{d\,(on)}$	Turn-On Delay Time	ALL	–	–	35*	ns	V_{DD} ≅ 95V, I_D = 19A, Z_o = 4.7Ω
t_r	Rise Time	ALL	–	–	100*	ns	(See Figs. 13 and 14)
$t_{d\,(off)}$	Turn-Off Delay Time	ALL	–	–	125*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	100*	ns	independent of operating temperature.)

THERMAL RESISTANCE

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
R_{thJC}	Junction-to-Case	ALL	–	–	0.83*	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

BODY-DRAIN DIODE RATINGS AND CHARACTERISTICS

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	2N6765	–	–	25*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		2N6766	–	–	30*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6765	–	–	50	A	
		2N6766	–	–	60		
V_{SD}	Diode Forward Voltage (1)	2N6765	0.85*	–	1.7*	V	T_C = 25°C, I_S = 25A, V_{GS} = 0
		2N6766	0.9*	–	1.8*	V	T_C = 25°C, I_S = 30A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	500	–	ns	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	10	–	μC	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs

*JEDEC registered values. (1) Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

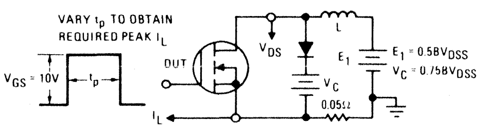


Fig. 1 — Clamped Inductive Test Circuit

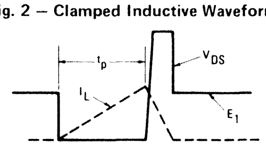


Fig. 2 — Clamped Inductive Waveforms

Fig. 3 — Typical Output Characteristics

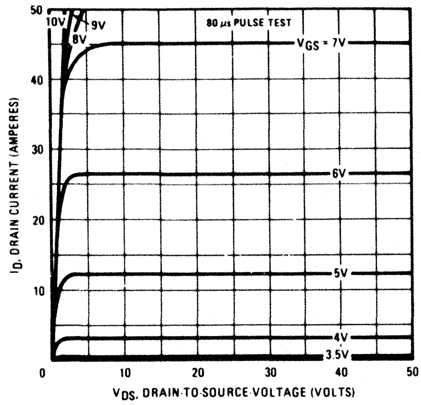


Fig. 4 — Typical Transfer Characteristics

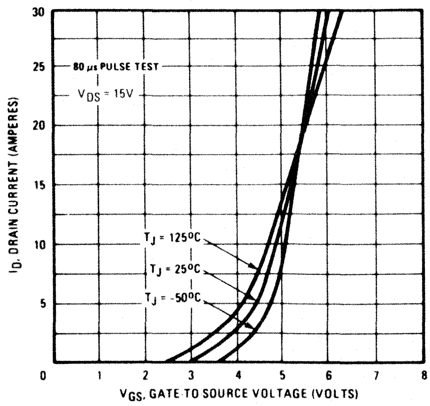


Fig. 5— Typical Saturation Characteristics (2N6765)

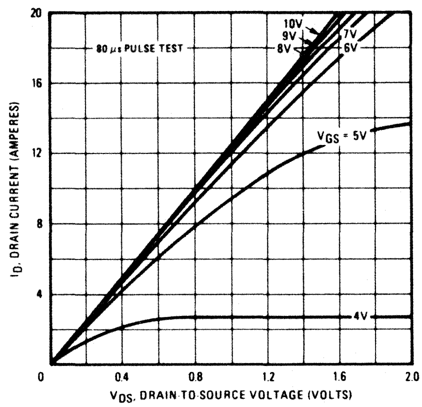


Fig. 6— Typical Saturation Characteristics (2N6766)

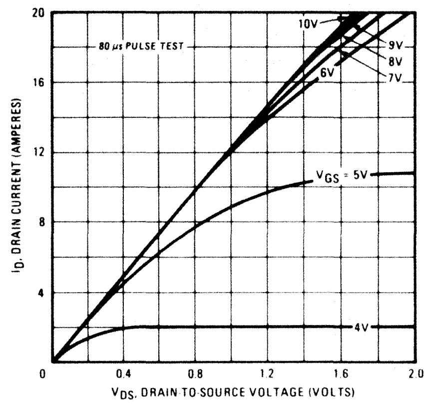


Fig. 7 — Typical Transconductance Vs. Drain Current

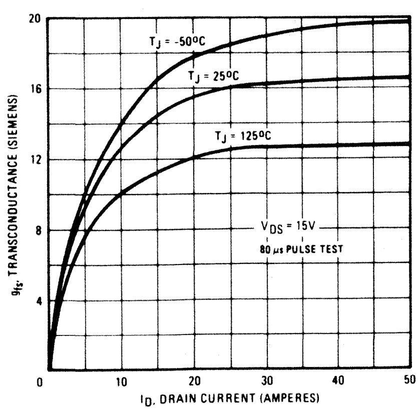


Fig. 8 — Maximum Safe Operating Area

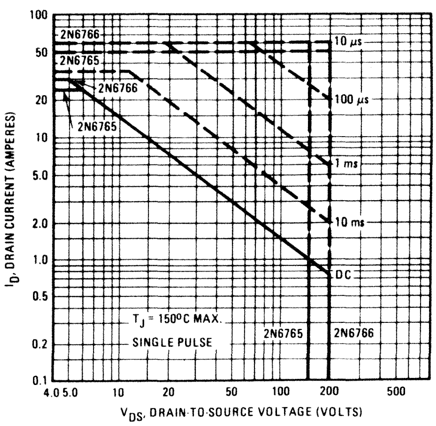


Fig. 9 – Normalized Typical On-Resistance Vs. Temperature

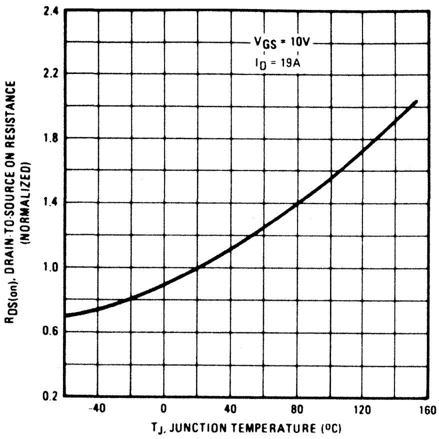


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

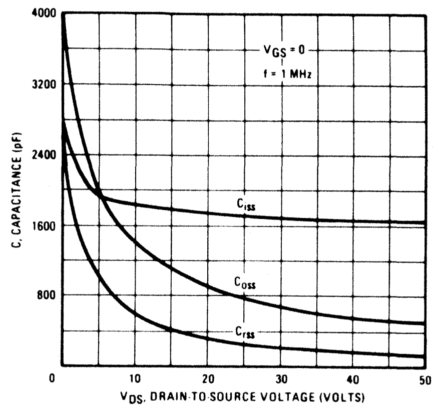


Fig. 11 – Power Vs. Temperature Derating Curve

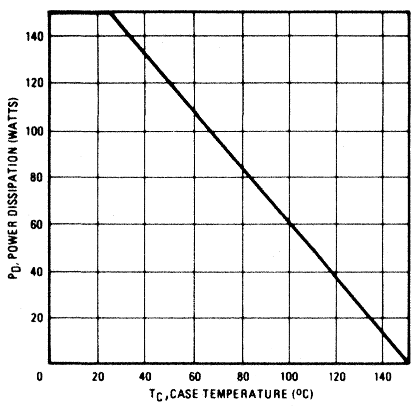


Fig. 12 – Typical Body-Drain Diode Forward Voltage

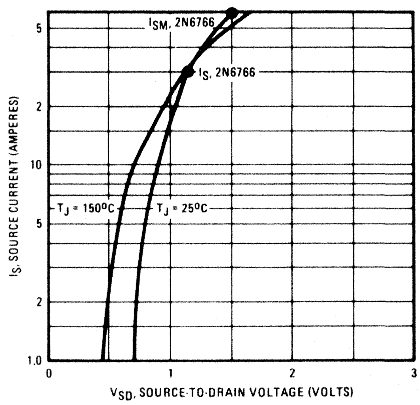


Fig. 13 – Switching Time Test Circuit

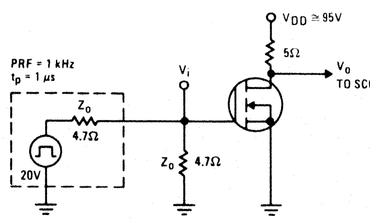
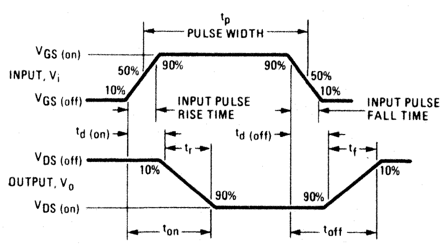


Fig. 14 – Switching Time Waveforms



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POWER MOSFET TRANSISTORS

400 Volt, 0.3 Ohm
N-Channel

2N6767
2N6768

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

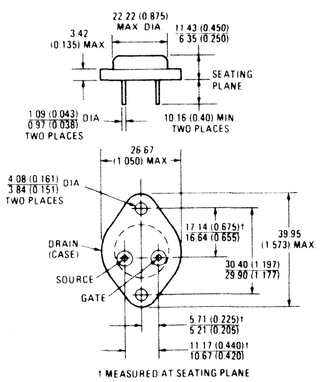
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6767	350V	0.4Ω	12A
2N6768	400V	0.3Ω	14A

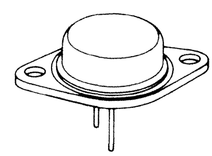
MECHANICAL SPECIFICATIONS

2N6767 2N6768



Dimensions in Millimeters and (Inches)

TO-3



UNITRODE

ABSOLUTE MAXIMUM RATINGS

Parameter		2N6767	2N6768	Units
V_{DS}	Drain – Source Voltage	350*	400*	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 1 MΩ)	350*	400*	V
I_D @ T_C = 25°C	Continuous Drain Current	12*	14*	A
I_D @ T_C = 100°C	Continuous Drain Current	7.75*	9.0*	A
I_{DM}	Pulsed Drain Current	20	25	A
V_{GS}	Gate – Source Voltage	±20*		V
P_D @ T_C = 25°C	Max. Power Dissipation	150* (See Fig. 11)		W
P_D @ T_C = 100°C	Max. Power Dissipation	60* (See Fig. 11)		W
	Linear Derating Factor	1.2* (See Fig. 11)		W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 µH 20	25	A
T_J T_{stg}	Operating and Storage Temperature Range	-55* to 150*		°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6767	350	–	–	V	V_{GS} = 0
		2N6768	400	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage (1)	2N6767	–	–	5.4*	V	V_{GS} = 10V, I_D = 12A
		2N6768	–	–	5.6*	V	V_{GS} = 10V, I_D = 14A
$R_{DS(on)}$	Static Drain-Source On-State Resistance (1)	2N6767	–	0.3	0.4*	Ω	V_{GS} = 10V, I_D = 7.75A
		2N6768	–	0.25	0.3*	Ω	V_{GS} = 10V, I_D = 9.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance (1)	2N6767	–	–	0.88*	Ω	V_{GS} = 10V, I_D = 7.75A, T_C = 125°C
		2N6768	–	–	0.66*	Ω	V_{GS} = 10V, I_D = 9.0A, T_C = 125°C
g_{fs}	Forward Transconductance (1)	ALL	8.0*	11.0	24*	S (℧)	V_{DS} = 15V, I_D = 9.0A
C_{iss}	Input Capacitance	ALL	1000*	2000	3000*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	200*	400	600*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	50*	100	200*	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	–	–	35*	ns	V_{DD} ≅ 180V, I_D = 9.0A, Z_o = 4.7Ω
t_r	Rise Time	ALL	–	–	65*	ns	(See Figs. 13 and 14)
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	–	–	150*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	75*	ns	independent of operating temperature.)

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	0.83*	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

BODY-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	2N6767	–	–	12*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		2N6768	–	–	14*	A	
I_{SM}	Pulsed Source Current (Body Diode)	2N6767	–	–	20	A	
		2N6768	–	–	25	A	
V_{SD}	Diode Forward Voltage (1)	2N6767	0.8*	–	1.6*	V	T_C = 25°C, I_S = 12A, V_{GS} = 0
		2N6768	0.85*	–	1.7*	V	T_C = 25°C, I_S = 14A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	1000	–	ns	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/µs
Q_{RR}	Reverse Recovered Charge	ALL	–	25	–	µC	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/µs

*JEDEC registered values. (1) Pulse Test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%

Fig. 1 — Clamped Inductive Test Circuit

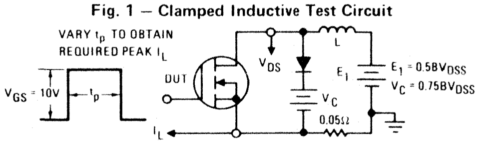


Fig. 2 — Clamped Inductive Waveforms

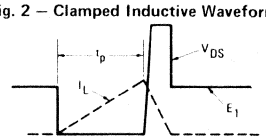


Fig. 3 — Typical Output Characteristics

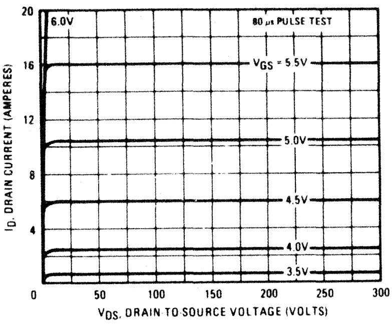


Fig. 4 — Typical Transfer Characteristics

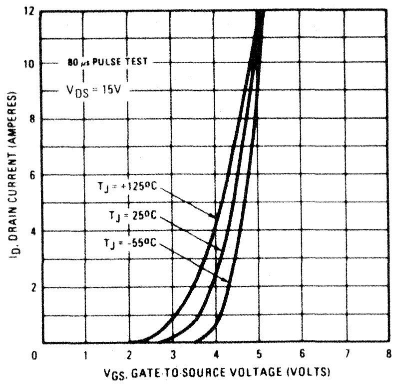


Fig. 5— Typical Saturation Characteristics (2N6767)

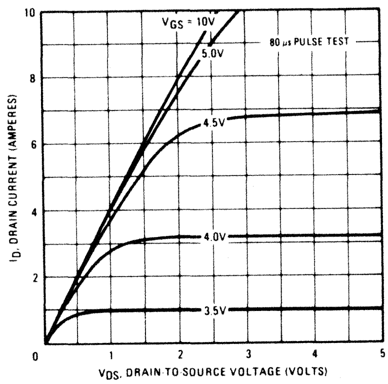


Fig. 6— Typical Saturation Characteristics (2N6768)

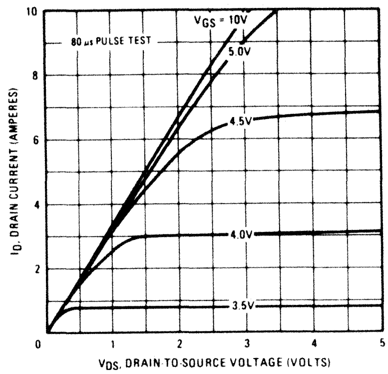


Fig. 7 — Typical Transconductance Vs. Drain Current

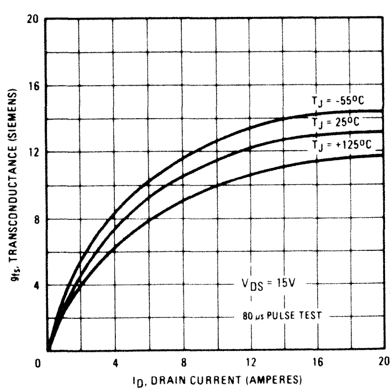


Fig. 8 — Maximum Safe Operating Area

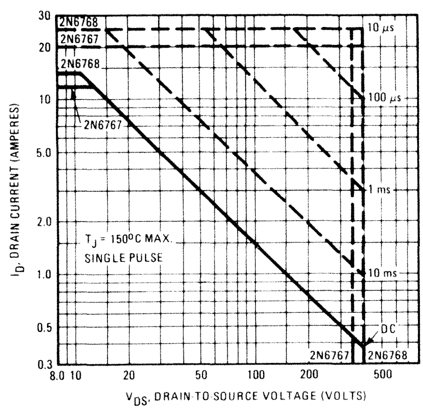


Fig. 9 — Normalized Typical On-Resistance Vs. Temperature

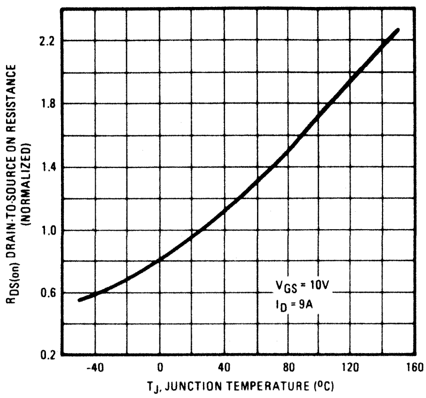


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

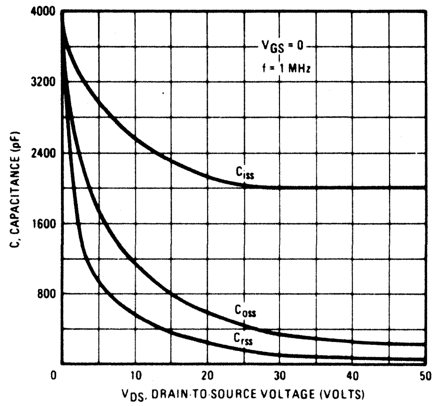


Fig. 11 — Power Vs. Temperature Derating Curve

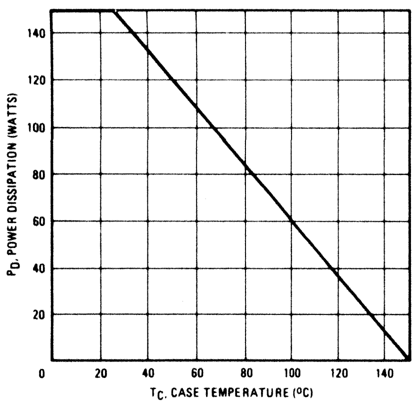


Fig. 12 — Typical Body-Drain Diode Forward Voltage

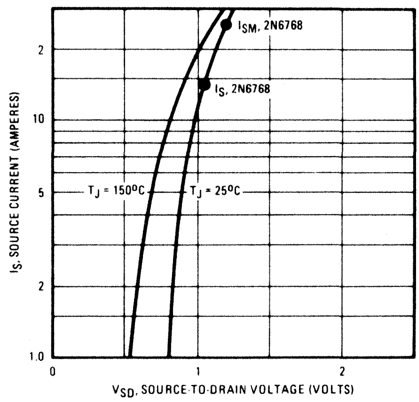


Fig. 13 — Switching Time Test Circuit

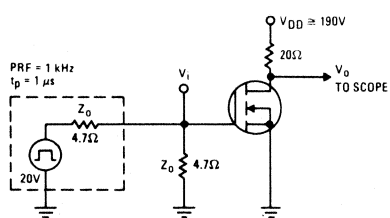
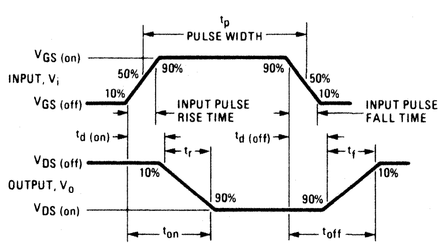


Fig. 14 — Switching Time Waveforms



POWER MOSFET TRANSISTORS

2N6769
2N6770

500 Volt, 0.4 Ohm
N-Channel

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

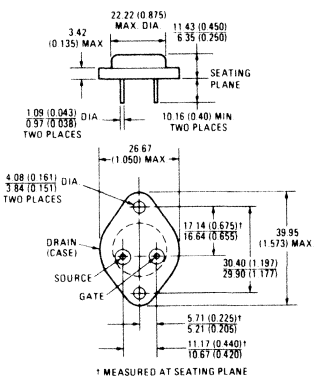
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6769	450V	0.5Ω	11A
2N6770	500V	0.4Ω	12A

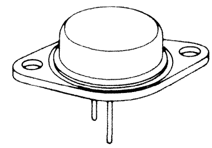
MECHANICAL SPECIFICATIONS

2N6769 2N6770



Dimensions in Millimeters and (Inches)

TO-3



UNITRODE

ABSOLUTE MAXIMUM RATINGS

Parameter		2N6769	2N6770	Units
V_{DS}	Drain – Source Voltage	450*	500*	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 1 MΩ)	450*	500*	V
I_D @ T_C = 25°C	Continuous Drain Current	11*	12*	A
I_D @ T_C = 100°C	Continuous Drain Current	7.0*	7.75*	A
I_{DM}	Pulsed Drain Current	20	25	A
V_{GS}	Gate – Source Voltage	±20*		V
P_D @ T_C = 25°C	Max. Power Dissipation	150* (See Fig. 11)		W
P_D @ T_C = 100°C	Max. Power Dissipation	60* (See Fig. 11)		W
	Linear Derating Factor	1.2* (See Fig. 11)		W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH 20	25	A
T_J T_{stg}	Operating and Storage Temperature Range	-55* to 150*		°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C

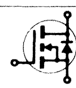
ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6769	450	–	–	V	V_{GS} = 0
		2N6770	500	–	–	V	I_D = 4.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = 0.8 x Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 25°C to 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage (1)	2N6769	–	–	6.0*	V	
		2N6770	–	–	6.0*	V	
$R_{DS(on)}$	Static Drain-Source On-State Resistance (1)	2N6769	–	0.4	0.5*	Ω	V_{GS} = 10V, I_D = 7.0A
		2N6770	–	0.3	0.4*	Ω	V_{GS} = 10V, I_D = 7.75A
$R_{DS(on)}$	Static Drain-Source On-State Resistance (1)	2N6769	–	–	1.1*	Ω	V_{GS} = 10V, I_D = 7.0A, T_C = 125°C
		2N6770	–	–	0.88*	Ω	V_{GS} = 10V, I_D = 7.75A, T_C = 125°C
g_{fs}	Forward Transconductance (1)	ALL	8.0*	12.0	24*	S (℧)	V_{DS} = 15V, I_D = 7.75A
C_{iss}	Input Capacitance	ALL	1000*	2000	3000*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	200*	400	600*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	50*	100	200*	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	–	–	35*	ns	V_{DD} ≅ 210V, I_D = 7.75A, Z_o = 4.7Ω
t_r	Rise Time	ALL	–	–	50*	ns	(See Figs. 13 and 14)
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	–	–	150*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	70*	ns	independent of operating temperature.)

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	0.83*	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

BODY-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	2N6769	–	–	11*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		2N6770	–	–	12*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6769	–	–	20	A	
		2N6770	–	–	25		
V_{SD}	Diode Forward Voltage (1)	2N6769	0.75*	–	1.5*	V	T_C = 25°C, I_S = 11A, V_{GS} = 0
		2N6770	0.80*	–	1.6*	V	T_C = 25°C, I_S = 12A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	400	–	ns	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	10	–	μC	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs

*JEDEC registered values. (1) Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

Fig. 1 — Clamped Inductive Test Circuit

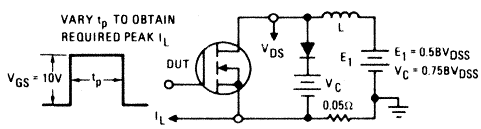


Fig. 2 — Clamped Inductive Waveforms

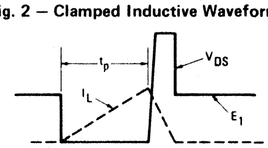


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Fig. 3 — Typical Output Characteristics

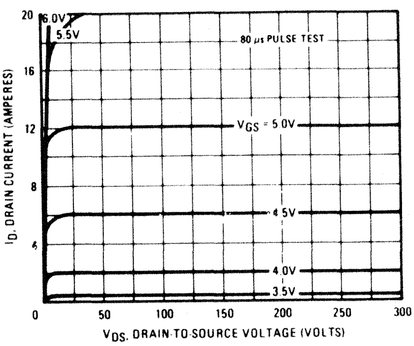


Fig. 4 — Typical Transfer Characteristics

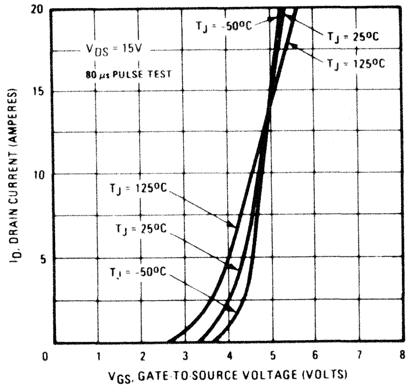


Fig. 5— Typical Saturation Characteristics (2N6769)

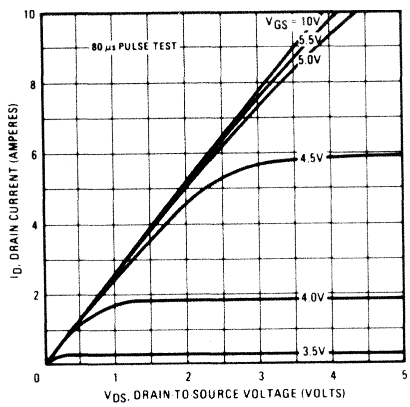


Fig. 6— Typical Saturation Characteristics (2N6770)

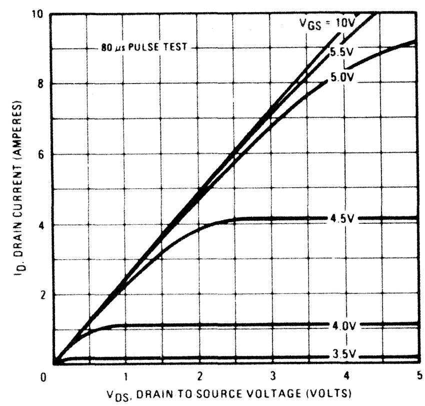


Fig. 7 — Typical Transconductance Vs. Drain Current

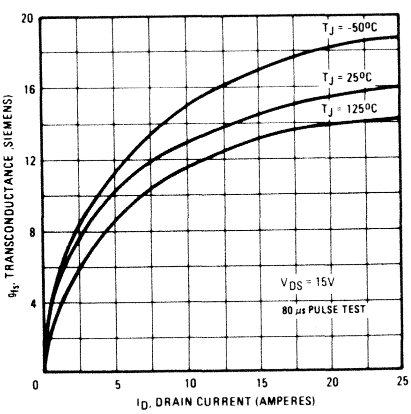


Fig. 8 — Maximum Safe Operating Area

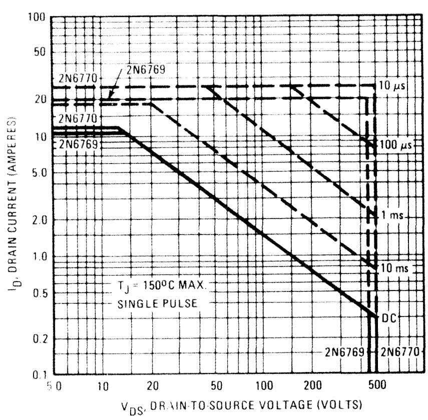


Fig. 9 — Normalized Typical On-Resistance Vs. Temperature

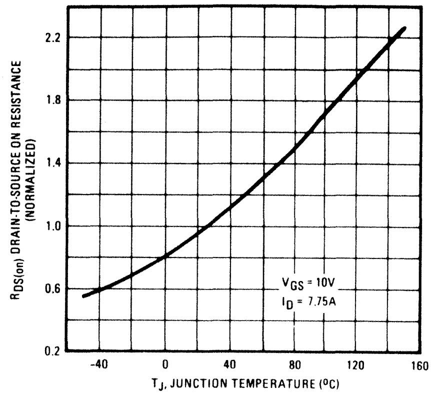


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

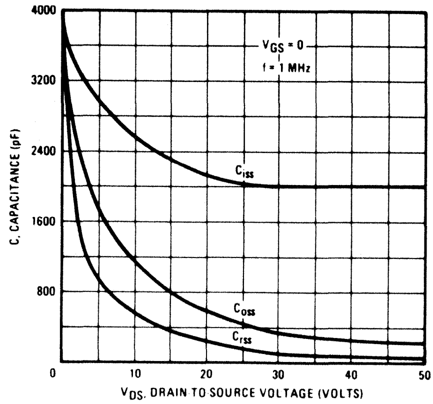


Fig. 11 — Power Vs. Temperature Derating Curve

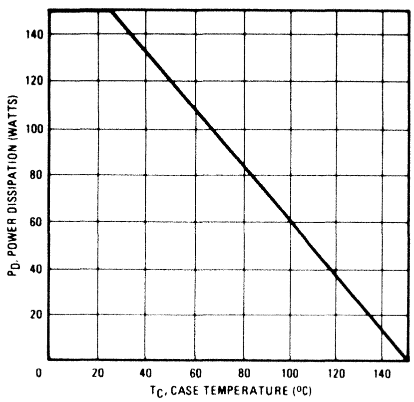


Fig. 12 — Typical Body-Drain Diode Forward Voltage

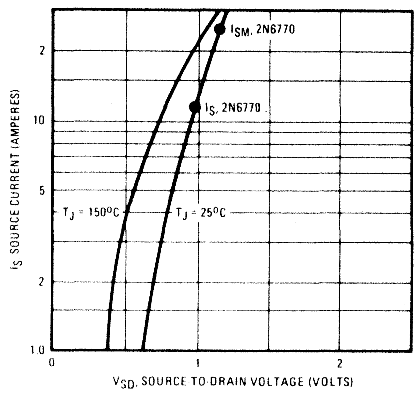


Fig. 13 — Switching Time Test Circuit

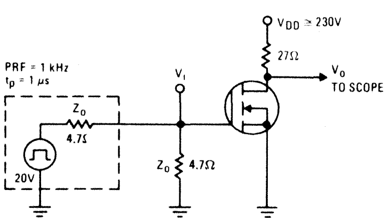
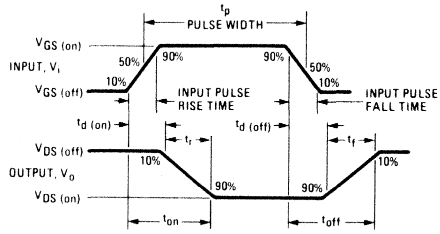


Fig. 14 — Switching Time Waveforms



POWER MOSFET TRANSISTORS

UFNA11
UFNA12

100 Volt, 1.5 Ohm
N-Channel

FEATURES

- Designed for High-Speed Switching Applications
- Direct Logic Interface
- No Thermal Runaway or Second Breakdown
- Economical Plastic Molded Construction

DESCRIPTION

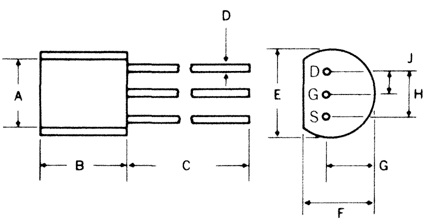
Near infinite gain, low on-state impedance and ultra fast switching speeds make the Unitrode POWER MOSFET ideally suited for many high-speed switching applications.

ABSOLUTE MAXIMUM RATINGS

	UFNA11	UFNA12
Drain-Source Voltage, V_{DS}	60V	100V
Drain-Gate Voltage, V_{DG}	60V	100V
Continuous Drain Current, I_D		1.0A
Pulsed Drain Current, I_{DM}		2.0A
Gate-Source Voltage, V_{GS}		±20V
Power Dissipation, P_D		
25°C Case		2.4W
25°C Ambient		750mW
Thermal Resistance, θ_{J-C}		62.5°C/W
Thermal Resistance, θ_{J-A}		200°C/W
Operating and Storage Temperature Range		−40°C to +150°C
Maximum Junction Temperature		+175°C

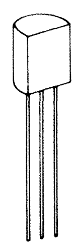
MECHANICAL SPECIFICATIONS

UFNA11 UFNA12



	INCHES	MILLIMETERS
A	.135 MIN.	3.42 MIN.
B	.170 - .210	4.31 - 5.33
C	.500 MIN.	12.70 MIN.
D	.016 - .019	.406 - .482
E	.175 - .205	4.44 - 5.21
F	.125 - .165	3.17 - 4.19
G	.080 - .105	2.03 - 2.66
H	.095 - .105	2.41 - 2.66
J	.045 - .055	1.14 - 1.40

TO-92

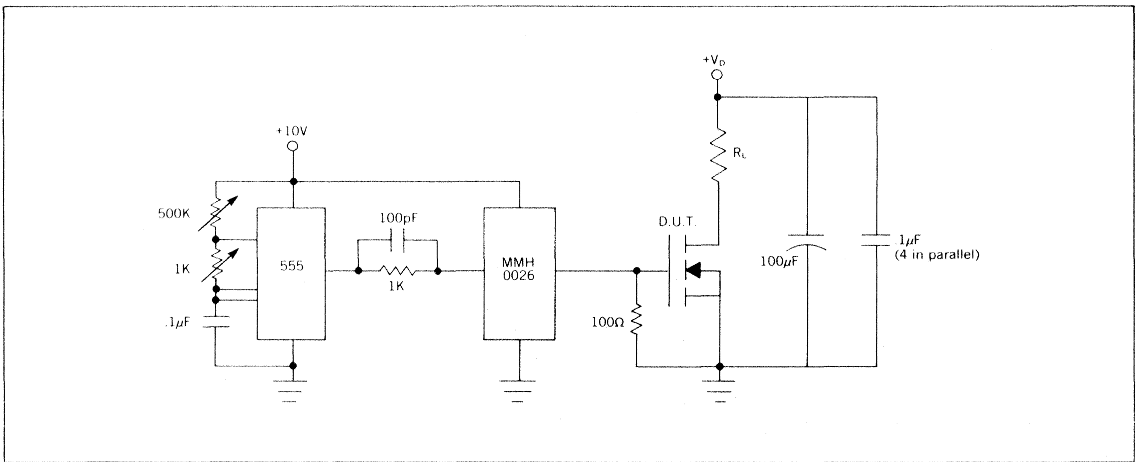


ELECTRICAL SPECIFICATIONS (at 25°C unless otherwise noted)

PARAMETER	SYMBOL	MIN.	MAX.	UNITS	TEST CONDITIONS
Drain-Source Breakdown Voltage UFNA11 UFNA12	 BV_{DSS} BV_{DSS}	 60 100	 — —	V	$V_{GS} = 0$ $I_D = 200\mu A$
Gate Threshold Voltage	$V_{GS(th)}$	2.0	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
Gate-Body Leakage	I_{GSS}	—	100	nA	$V_{GS} = 10V$, $V_{DS} = 0$
Zero Gate Voltage Drain Current	I_{DSS}	—	10	μA	$V_{DS} = 0.8$ Rating, $V_{GS} = 0$
		—	500	μA	$V_{DS} = 0.8$ Rating, $V_{GS} = 0$ $T_J = 125°C$
On-State Drain Current	$I_{D(on)}$	2.0	—	A	$V_{DS} = 25V$, $V_{GS} = 10V$ (Note 1)
Drain-Source On-State Resistance	$R_{DS(on)}$	—	1.5	Ω	$V_{GS} = 10V$, $I_D = 1.0A$ (Note 1)
Forward Transconductance	g_{fs}	400	—	m℧	$V_{DS} = 25V$, $I_D = 1A$ (Note 1)
Input Capacitance	C_{iss}	—	200	pF	$V_{GS} = 0$ $V_{DS} = 25V$ f = 1.0MHz
Output Capacitance	C_{oss}	—	80	pF	
Reverse Transfer Capacitance	C_{rss}	—	40	pF	
Turn-On Delay Time	$t_{d(on)}$	—	10	ns	$V_D \approx .5 \times$ Rated V_{DS} $I_D = .5A$ $V_{GS(on)} = 10V$ (See Test Circuit Below)
Rise Time	t_r	—	10	ns	
Turn-Off Delay Time	$t_{d(off)}$	—	20	ns	
Fall-Time	t_f	—	20	ns	

Note: 1. Pulse width = 300μs; Duty Cycle ≤ 2%

SWITCHING SPEED CIRCUIT



POWER MOSFET TRANSISTORS

100 Volt, 2.4 Ohm
N-Channel

UFND1Z0
UFND1Z1
UFND1Z2
UFND1Z3

FEATURES

- For Automatic Insertion
- Compact, End Stackable
- Fast Switching
- Low Drive Current
- Easily Paralleled
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

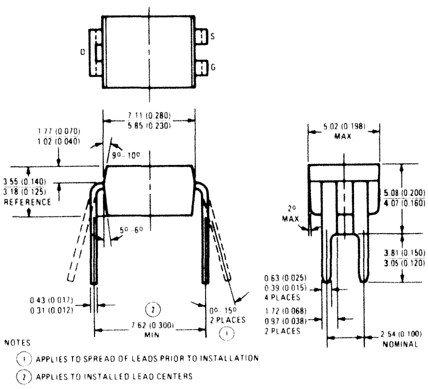
When packaged in the low profile, end stackable 4 pin dual-in-line package, the Unitrode power MOSFET devices can be used in high volume applications where automatic insertion is a must such as computer circuit boards, telecommunication equipment, consumer equipment, and printers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFND1Z0	100V	2.4Ω	0.5A
UFND1Z1	60V	2.4Ω	0.5A
UFND1Z2	100V	3.2Ω	0.4A
UFND1Z3	60V	3.2Ω	0.4A

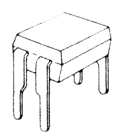
MECHANICAL SPECIFICATIONS

UFND1Z0 UFND1Z1 UFND1Z2 UFND1Z3



Nominal Dimensions in Millimeters and (Inches)

DIL-4

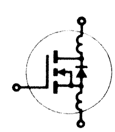


UNITRODE

ABSOLUTE MAXIMUM RATINGS

Parameter		UFND1Z0	UFND1Z1	UFND1Z2	UFND1Z3	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	0.5	0.5	0.4	0.4	A
I_{DM}	Pulsed Drain Current	2.0	2.0	1.5	1.5	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	1.0 (See Fig. 13)				W
	Linear Derating Factor	0.008 (See Fig. 13)				W/K
I_{LM}	Inductive Current, Clamped (See Fig. 14 and 15) L = 100μH	2.0	2.0	1.5	1.5	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C

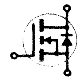
ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFND1Z0 UFND1Z2	100	—	—	V	V_{GS} = 0V
		UFND1Z1 UFND1Z3	60	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFND1Z0 UFND1Z1	0.5	—	—	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		UFND1Z2 UFND1Z3	0.4	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFND1Z0 UFND1Z1	—	2.2	2.4	Ω	V_{GS} = 10V, I_D = 0.25A
		UFND1Z2 UFND1Z3	—	2.8	3.2	Ω	
g_{fs}	Forward Transconductance ②	ALL	—	0.35	—	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 0.25A
C_{iss}	Input Capacitance	ALL	—	50	70	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 9
C_{oss}	Output Capacitance	ALL	—	20	30	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	5.0	10	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	10	20	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 0.25A, Z_O = 50Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	15	25	ns	
t_f	Fall Time	ALL	—	10	20	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	2.0	3.0	nC	V_{GS} = 10V, I_D = 1.2A, V_{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	1.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	1.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	4.0	—	nH	Measured from the drain lead, 2.0mm (0.08 in.) from package to center of die. / Modified MOSFET symbol showing the internal device inductances. 
L_S	Internal Source Inductance	ALL	—	6.0	—	nH	Measured from the source lead, 2.0mm (0.08 in.) from package to source bonding pad.

THERMAL RESISTANCE

R_{thJA}	Junction to Ambient	ALL	—		120	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFND1Z0 UFND1Z1	—	—	0.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFND1Z2 UFND1Z3	—	—	0.4	A	
I_{SM}	Pulse Source Current (Body Diode)	UFND1Z0 UFND1Z1	—	—	2.0	A	
		UFND1Z2 UFND1Z3	—	—	1.5	A	
V_{SD}	Diode Forward Voltage ②	UFND1Z0 UFND1Z1	—	—	1.4	V	T_C = 25°C, I_S = 0.5A, V_{GS} = 0V
		UFND1Z2 UFND1Z3	—	—	1.3	V	T_C = 25°C, I_S = 0.4A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	100	—	ns	T_J = 150°C, I_F = 0.5A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	0.2	—	μC	T_J = 150°C, I_F = 0.5A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

Fig. 1 — Typical Output Characteristics

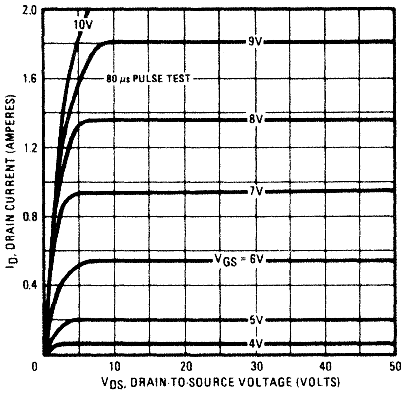


Fig. 2 — Typical Transfer Characteristics

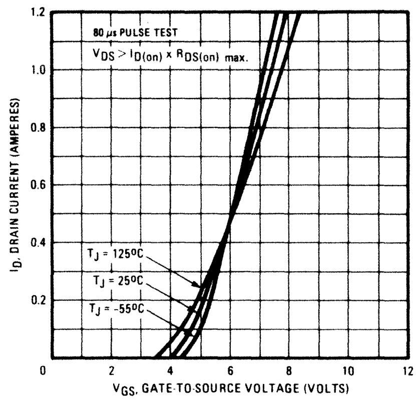


Fig. 3 — Typical Saturation Characteristics

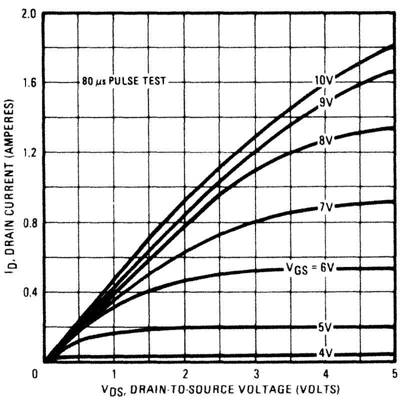


Fig. 4 — Maximum Safe Operating Area

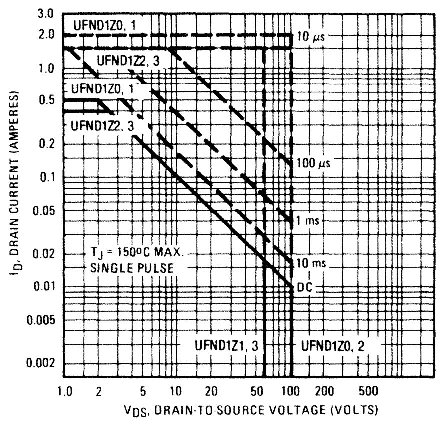


Fig. 5 — Typical Transconductance Vs. Drain Current

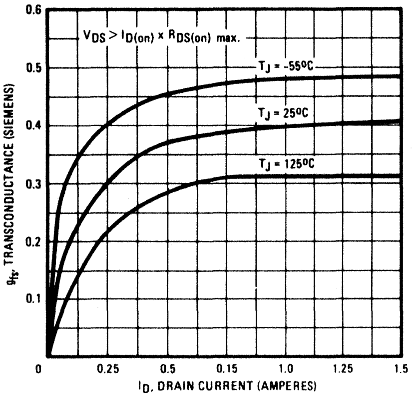


Fig. 6 — Typical Source-Drain Diode Forward Voltage

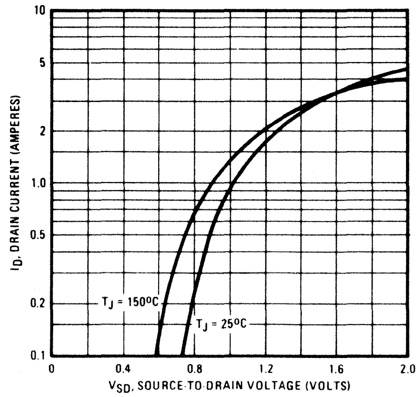


Fig. 7 — Breakdown Voltage Vs. Temperature

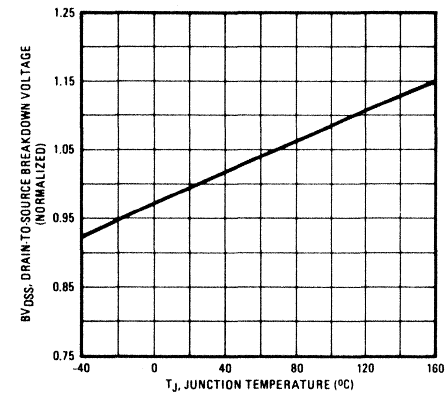


Fig. 8 — Normalized On-Resistance Vs. Temperature

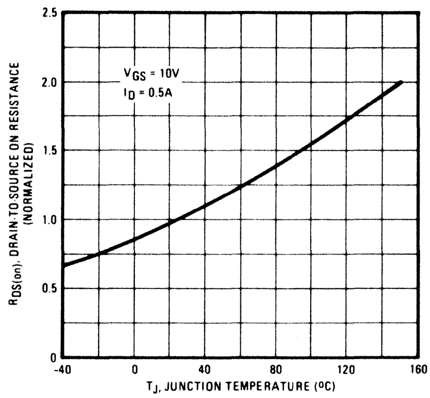


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

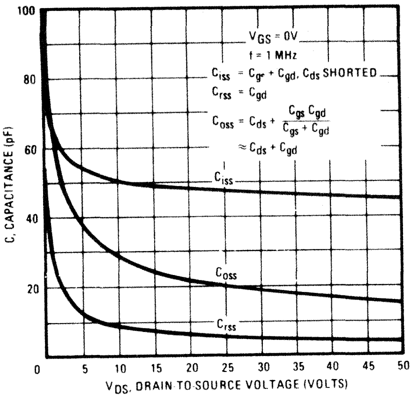


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

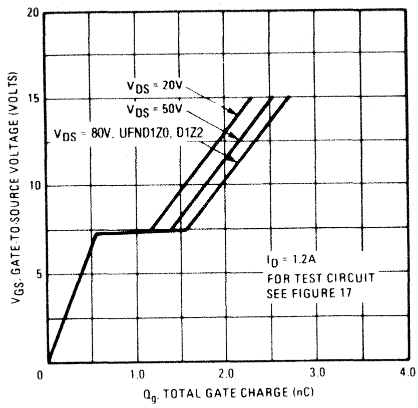


Fig. 11 — Typical On-Resistance Vs. Drain Current

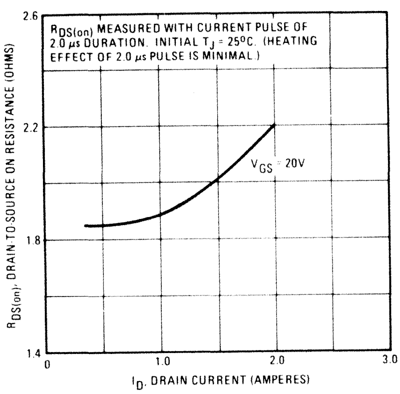


Fig. 12 — Maximum Drain Current Vs. Case Temperature

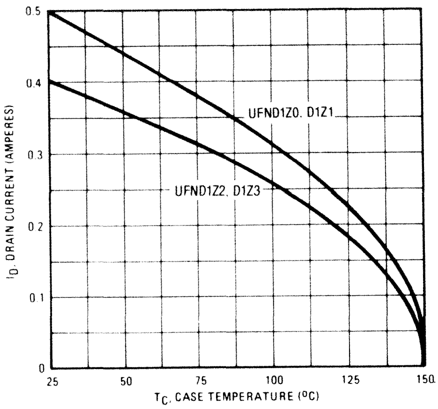


Fig. 13 — Power Vs. Temperature Derating Curve

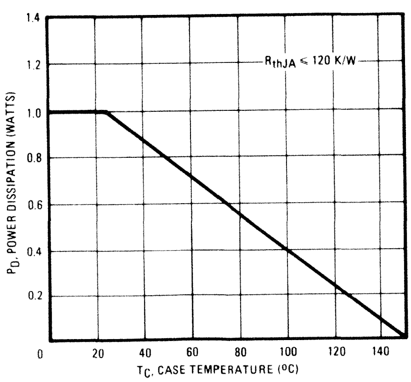


Fig. 14 — Clamped Inductive Test Circuit

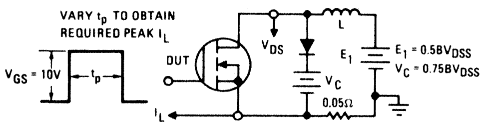


Fig. 15 — Clamped Inductive Waveforms

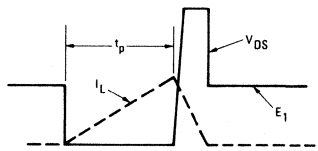


Fig. 16 — Switching Time Test Circuit

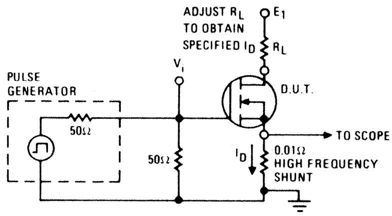
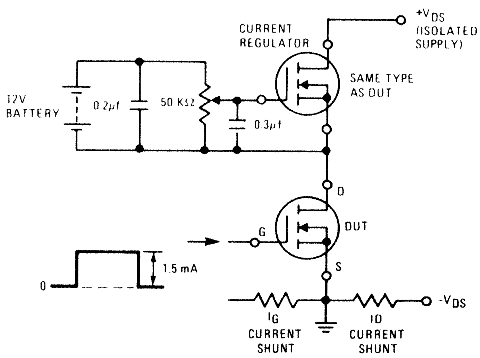


Fig. 17 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

100 Volt, 0.6 Ohm
N-Channel

UFND110
UFND111
UFND112
UFND113

FEATURES
- For Automatic Insertion
- Compact, End Stackable
- Fast Switching
- Low Drive Current
- Easily Paralleled
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

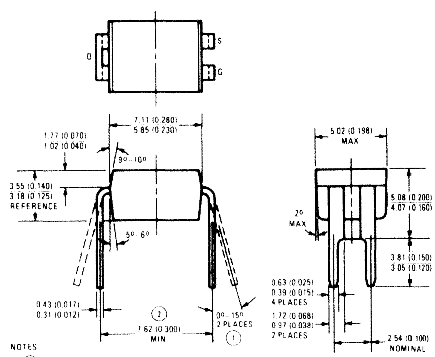
When packaged in the low profile, end stackable 4 pin dual-in-line package, the Unitrode power MOSFET devices can be used in high volume applications where automatic insertion is a must such as computer circuit boards, consumer equipment, and printers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFND110	100V	0.6Ω	1.0A
UFND111	60V	0.6Ω	1.0A
UFND112	100V	0.8Ω	0.8A
UFND113	60V	0.8Ω	0.8A

MECHANICAL SPECIFICATIONS

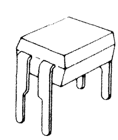
UFND110 UFND111 UFND112 UFND113



NOTES
① APPLIES TO SPREAD OF LEADS PRIOR TO INSTALLATION
② APPLIES TO INSTALLED LEAD CENTERS

Nominal Dimensions in Millimeters and (Inches)

DIL-4

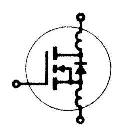


UNITRODE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	UFND110	UFND111	UFND112	UFND113	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	1.0	1.0	0.8	0.8	A
I_{DM}	Pulsed Drain Current	4.0	4.0	3.0	3.0	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	1.0 (See Fig. 13)				W
	Linear Derating Factor	0.008 (See Fig. 13)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 14 and 15) L = 100μH 4.0	4.0	3.0	3.0	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C

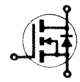
ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Symbol	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFND110 UFND112	100	–	–	V	V_{GS} = 0V
		UFND111 UFND113	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFND110 UFND111	1.0	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		UFND112 UFND113	0.8	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFND110 UFND111	–	0.5	0.6	Ω	V_{GS} = 10V, I_D = 0.8A
		UFND112 UFND113	–	0.6	0.8	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.8	1.2	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 0.8A
C_{iss}	Input Capacitance	ALL	–	135	200	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 9
C_{oss}	Output Capacitance	ALL	–	80	100	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	20	25	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	10	20	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 0.8A, Z_o = 50Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	15	25	ns	
t_f	Fall Time	ALL	–	10	20	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	5.0	7.0	nC	V_{GS} = 10V, I_D = 4.0A, V_{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	2.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	7.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	4.0	–	nH	Measured from the drain lead, 2.0mm (0.08 in.) from package to center of die. Modified MOSFET symbol showing the internal device inductances. 
L_S	Internal Source Inductance	ALL	–	6.0	–	nH	Measured from the source lead, 2.0mm (0.08 in.) from package to source bonding pad.

THERMAL RESISTANCE

Symbol	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
R_{thJA}	Junction-to-Ambient	ALL	–	–	120	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFND110 UFND111	—	—	1.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFND112 UFND113	—	—	0.8	A	
I_{SM}	Pulse Source Current (Body Diode)	UFND110 UFND111	—	—	4.0	A	
		UFND112 UFND113	—	—	3.0	A	
V_{SD}	Diode Forward Voltage ②	UFND110 UFND111	—	—	2.5	V	$T_C = 25°C, I_S = 1.0A, V_{GS} = 0V$
		UFND112 UFND113	—	—	2.0	V	$T_C = 25°C, I_S = 0.8A, V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	100	—	ns	$T_J = 150°C, I_F = 1.0A, dI_F/dt = 100\ A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	0.2	—	μC	$T_J = 150°C, I_F = 1.0A, dI_F/dt = 100\ A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25°C$ to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

Fig. 1 — Typical Output Characteristics

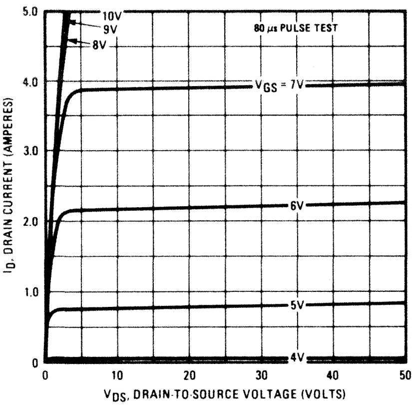


Fig. 2 — Typical Transfer Characteristics

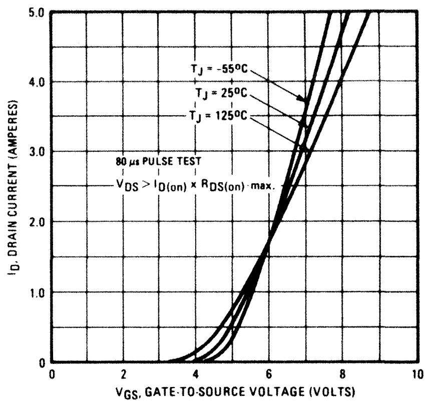


Fig. 3 — Typical Saturation Characteristics

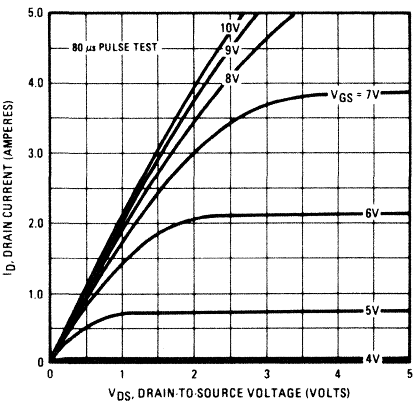


Fig. 4 — Maximum Safe Operating Area

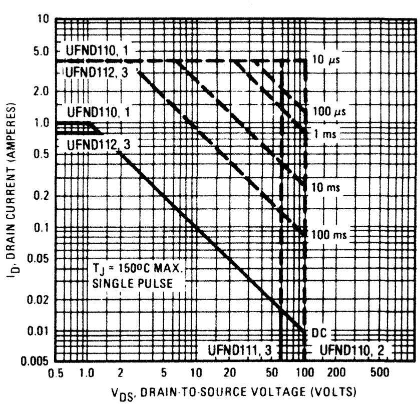


Fig. 5 — Typical Transconductance Vs. Drain Current

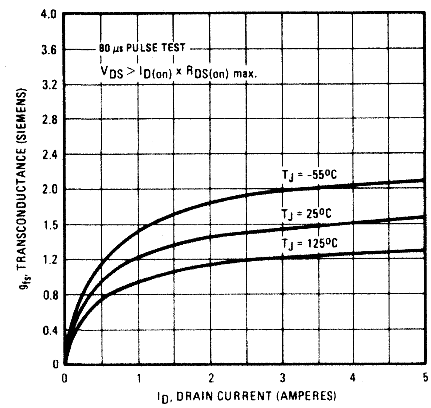


Fig. 6 — Typical Source-Drain Diode Forward Voltage

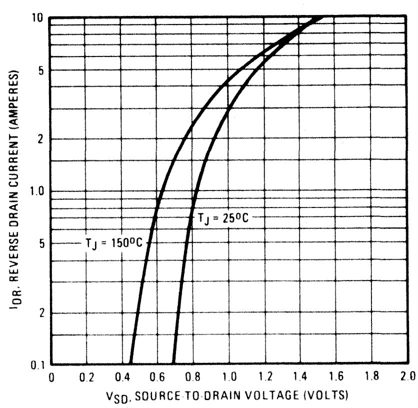


Fig. 7 — Breakdown Voltage Vs. Temperature

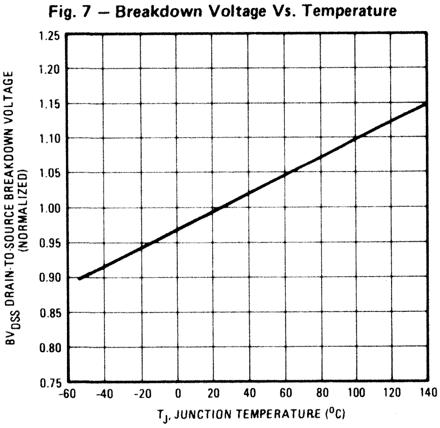


Fig. 8 — Normalized On-Resistance Vs. Temperature

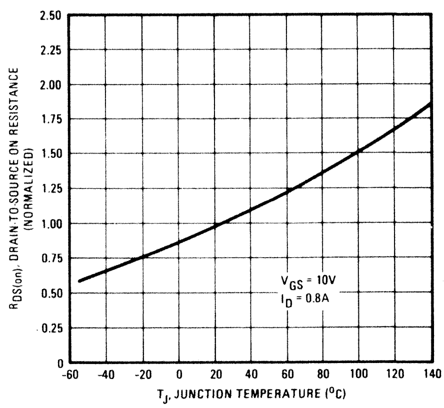


Fig. 9 – Typical Capacitance Vs. Drain-to-Source Voltage

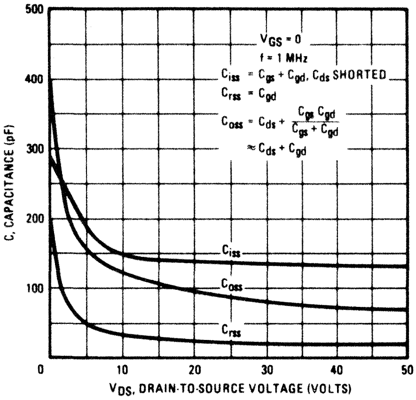


Fig. 10 – Typical Gate Charge Vs. Gate-to-Source Voltage

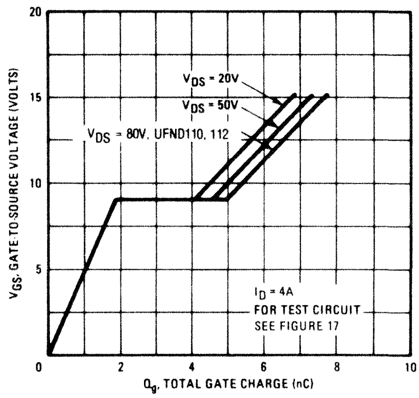


Fig. 11 – Typical On-Resistance Vs. Drain Current

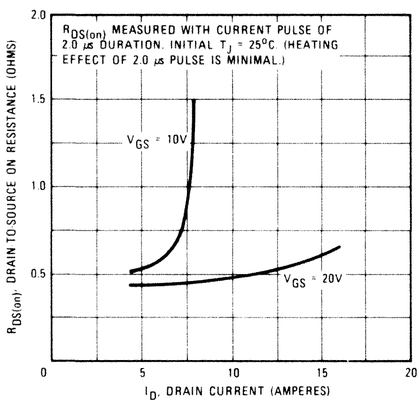


Fig. 12 – Maximum Drain Current Vs. Case Temperature

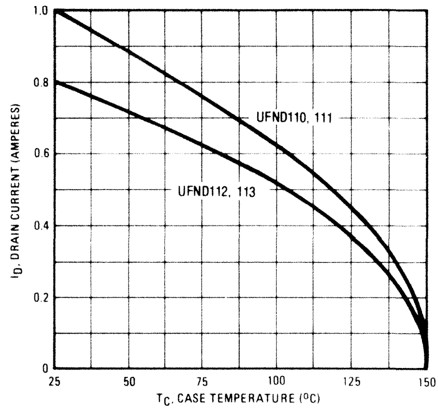


Fig. 13 – Power Vs. Temperature Derating Curve

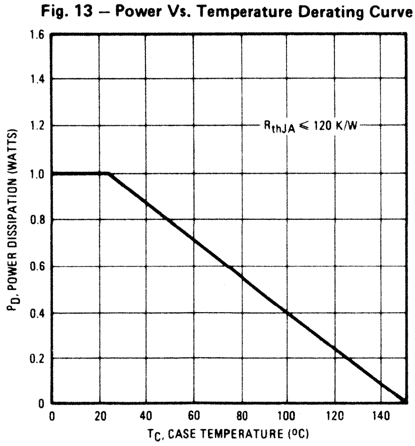


Fig. 14 — Clamped Inductive Test Circuit

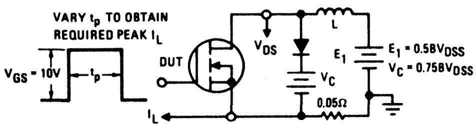


Fig. 15 — Clamped Inductive Waveforms

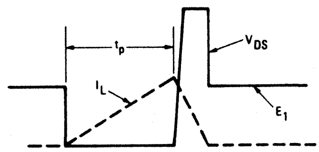


Fig. 16 — Switching Time Test Circuit

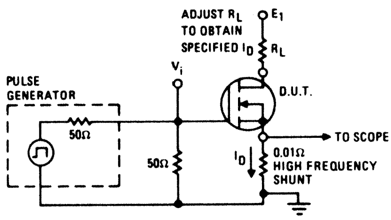
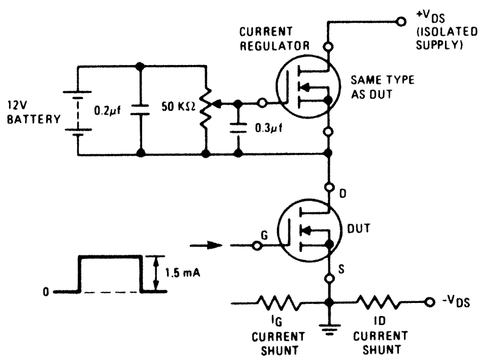


Fig. 17 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

100 Volt, 0.3 Ohm
N-Channel

UFND120
UFND123

FEATURES

- For Automatic Insertion
- Compact, End Stackable
- Fast Switching
- Low Drive Current
- Easily Paralleled
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

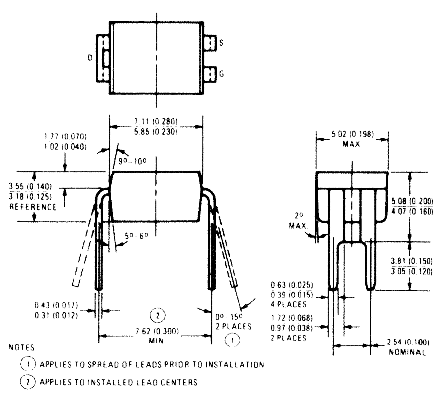
When packaged in the low profile, end stackable 4 pin dual-in-line package, the Unitrode power MOSFET devices can be used in high volume applications where automatic insertion is a must such as computer circuit boards, telecommunication equipment, consumer equipment, and printers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFND120	100V	0.3Ω	1.3A
UFND123	60V	0.4Ω	1.1A

MECHANICAL SPECIFICATIONS

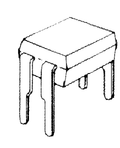
UFND120 UFND123



NOTES
(1) APPLIES TO SPREAD OF LEADS PRIOR TO INSTALLATION
(2) APPLIES TO INSTALLED LEAD CENTERS

Nominal Dimensions in Millimeters and (Inches)

DIL-4



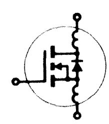
UNITRODE

ABSOLUTE MAXIMUM RATINGS

Parameter		UFND120	UFND123	Units
V_{DS}	Drain — Source Voltage ①	100	60	V
V_{DGR}	Drain — Gate Voltage (R_{GS} = 1 MΩ) ①	100	60	V
I_D @ T_A = 25°C	Continuous Drain Current	1.3	1.1	A
I_{DM}	Pulsed Drain Current	5.2	4.4	A
V_{GS}	Gate — Source Voltage	± 20		V
P_D @ T_A = 25°C	Max. Power Dissipation	1.0 (See Fig. 13)		W
	Linear Derating Factor	0.008 (See Fig. 13)		W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 14 and 15) L = 100μH 5.21	4.4	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150		°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)		°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain — Source Breakdown Voltage	UFND120	100	—	—	V	V_{GS} = 0V
		UFND123	60	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate — Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate — Source Leakage Reverse	ALL	—	—	−500	nA	V_{GS} = −20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFND120	1.3	—	—	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		UFND123	1.1	—	—	A	
$R_{DS(on)}$	Static Drain — Source On-State Resistance ②	UFND120	—	0.25	0.30	Ω	V_{GS} = 10V, I_D = 0.6A
		UFND123	—	0.30	0.40	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.9	1.0	—	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 0.6A
C_{iss}	Input Capacitance	ALL	—	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 9
C_{oss}	Output Capacitance	ALL	—	200	400	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	50	100	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	20	40	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 0.6A, Z_o = 50Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	35	70	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	50	100	ns	
t_f	Fall Time	ALL	—	35	70	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	11	15	nC	V_{GS} = 10V, I_D = 5.2A, V_{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	6.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	5.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	4.0	—	nH	Measured from the drain lead, 2.0mm (0.08 in.) from package to center of die. — Modified MOSFET symbol showing the internal device inductances.
L_S	Internal Source Inductance	ALL	—	6.0	—	nH	Measured from the source lead, 2.0mm (0.08 in.) from package to source bonding pad.



THERMAL RESISTANCE

R_{thJA}	Junction-to-Ambient	ALL	—	—	120	K/W	Free Air Operation

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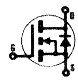
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFND120	—	—	1.3	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFND123	—	—	1.1	A	
I_{SM}	Pulse Source Current (Body Diode)	UFND120	—	—	5.2	A	
		UFND123	—	—	4.4	A	
V_{SD}	Diode Forward Voltage ②	UFND120	—	—	2.5	V	$T_C = 25°C$, $I_S = 1.3A$, $V_{GS} = 0V$
		UFND123	—	—	2.3	V	$T_C = 25°C$, $I_S = 1.1A$, $V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	280	—	ns	$T_J = 150°C$, $I_F = 1.3A$, $dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	1.6	—	μC	$T_J = 150°C$, $I_F = 1.3A$, $dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

①$T_J = 25°C$ to $150°C$. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

Fig. 1 — Typical Output Characteristics

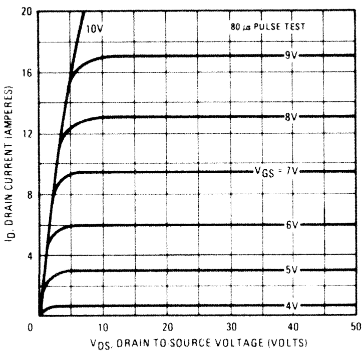


Fig. 2 — Typical Transfer Characteristics

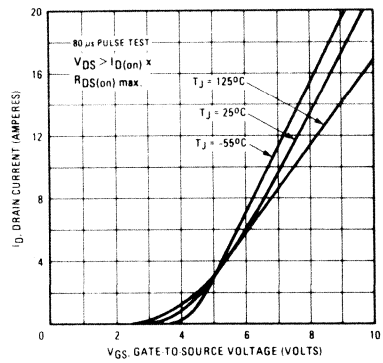


Fig. 3 — Typical Saturation Characteristics

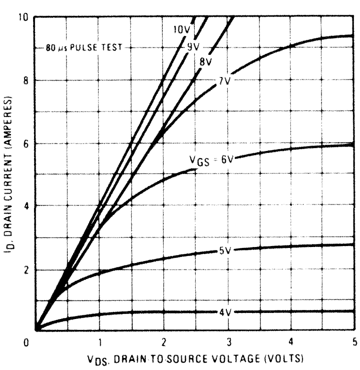


Fig. 4 — Maximum Safe Operating Area

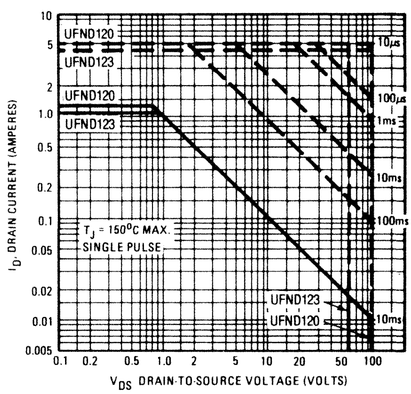


Fig. 5 — Typical Transconductance Vs. Drain Current

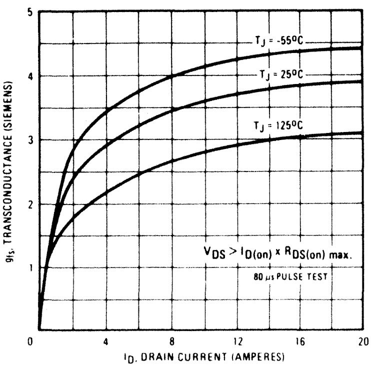


Fig. 6 — Typical Source-Drain Diode Forward Voltage

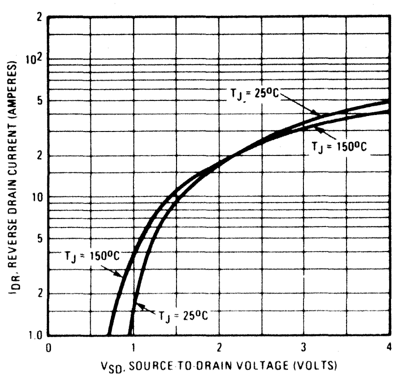


Fig. 7 — Breakdown Voltage Vs. Temperature

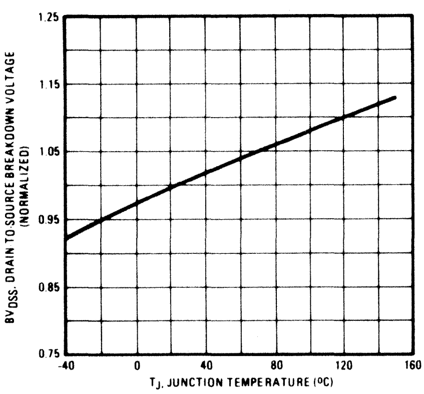


Fig. 8 — Normalized On-Resistance Vs. Temperature

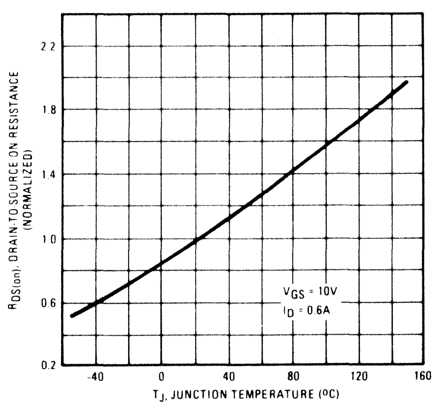


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Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

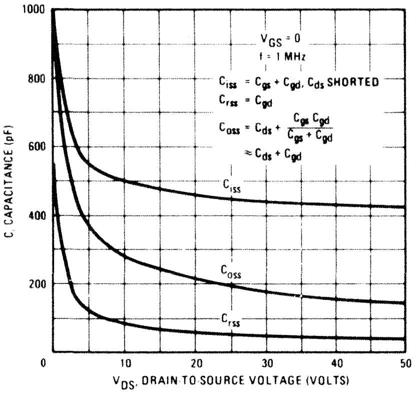


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

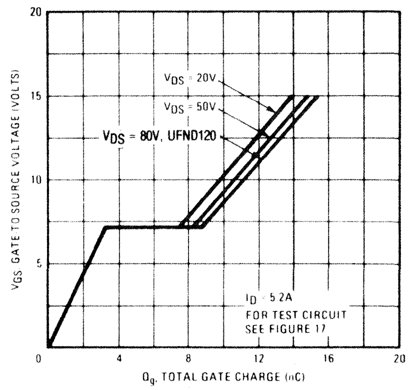


Fig. 11 — Typical On-Resistance Vs. Drain Current

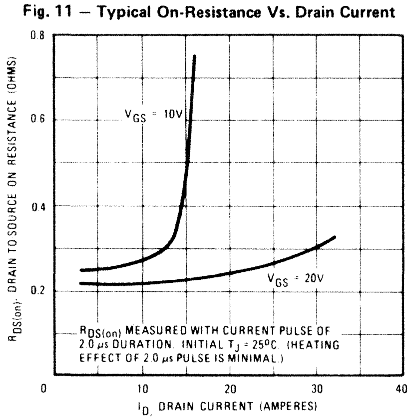


Fig. 12 — Maximum Drain Current Vs. Case Temperature

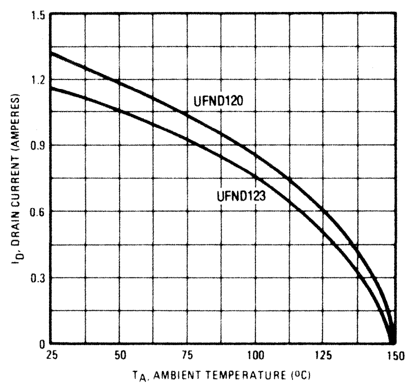


Fig. 13 — Power Vs. Temperature Derating Curve

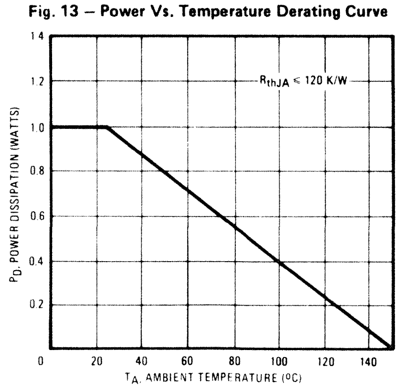


Fig. 14 – Clamped Inductive Test Circuit

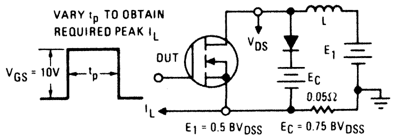


Fig. 15 – Clamped Inductive Waveforms

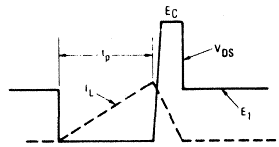


Fig. 16 – Switching Time Test Circuit

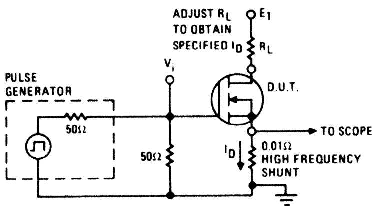
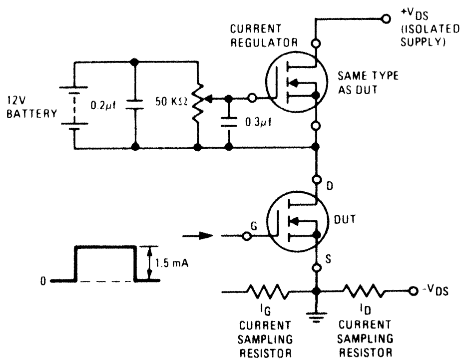


Fig. 17 – Gate Charge Test Circuit



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POWER MOSFET TRANSISTORS

UFND210
UFND213

200 Volt, 1.5 Ohm
N-Channel

FEATURES

- For Automatic Insertion
- Compact, End Stackable
- Fast Switching
- Low Drive Current
- Easily Paralleled
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

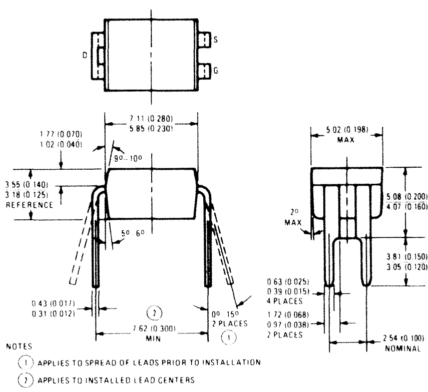
When packaged in the low profile, end stackable 4 pin dual-in-line package, the Unitrode power MOSFET devices can be used in high volume applications where automatic insertion is a must such as computer circuit boards, telecommunication equipment, consumer equipment, and printers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFND210	200V	1.5Ω	0.6A
UFND213	150V	2.4Ω	0.45A

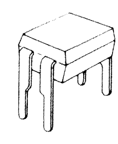
MECHANICAL SPECIFICATIONS

UFND210 UFND213



Nominal Dimensions in Millimeters and (Inches)

DIL-4



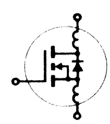
UNITRODE

ABSOLUTE MAXIMUM RATINGS

Parameter		UFND210	UFND213	Units
V_{DS}	Drain — Source Voltage ①	200	150	V
V_{DGR}	Drain — Gate Voltage (R_{GS} = 1 MΩ) ①	200	150	V
I_D @ T_A = 25°C	Continuous Drain Current	0.6	0.45	A
I_{DM}	Pulsed Drain Current	2.5	1.8	A
V_{GS}	Gate — Source Voltage	± 20		V
P_D @ T_A = 25°C	Max. Power Dissipation	1.0 (See Fig. 13)		W
	Linear Derating Factor	0.008 (See Fig. 13)		W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 14 and 15) L = 100μH 2.5	1.8	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150		°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)		°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

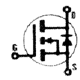
Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain — Source Breakdown Voltage	UFND210	200	—	—	V	V_{GS} = 0V
		UFND213	150	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate — Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate — Source Leakage Reverse	ALL	—	—	−500	nA	V_{GS} = −20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFND210	0.6	—	—	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		UFND213	0.45	—	—	A	
$R_{DS(on)}$	Static Drain — Source On-State Resistance ②	UFND210	—	1.0	1.5	Ω	V_{GS} = 10V, I_D = 0.3A
		UFND213	—	1.5	2.4	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.5	0.8	—	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 0.3A
C_{iss}	Input Capacitance	ALL	—	135	150	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 9
C_{oss}	Output Capacitance	ALL	—	60	80	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	16	25	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	8.0	15	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 0.3A, Z_o = 50Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	10	15	ns	
t_f	Fall Time	ALL	—	8.0	15	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	5.0	7.5	nC	V_{GS} = 10V, I_D = 2.5A, V_{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	2.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	3.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	4.0	—	nH	Measured from the drain lead, 2.0mm (0.08 in.) from package to center of die. — Modified MOSFET symbol showing the internal device inductances.
L_S	Internal Source Inductance	ALL	—	6.0	—	nH	Measured from the source lead, 2.0mm (0.08 in.) from package to source bonding pad.



THERMAL RESISTANCE

R_{thJA}	Junction-to-Ambient	ALL	—	—	120	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFND210	—	—	0.6	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFND213	—	—	0.45	A	
I_{SM}	Pulse Source Current (Body Diode)	UFND210	—	—	2.5	A	
		UFND213	—	—	1.8	A	
V_{SD}	Diode Forward Voltage ②	UFND210	—	—	2.0	V	$T_A = 25°C, I_S = 0.6A, V_{GS} = 0V$
		UFND213	—	—	1.8	V	$T_A = 25°C, I_S = 0.45A, V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	290	—	ns	$T_J = 150°C, I_F = 0.6A, dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	2.0	—	μC	$T_J = 150°C, I_F = 0.6A, dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25°C$ to $150°C$. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

Fig. 1 — Typical Output Characteristics

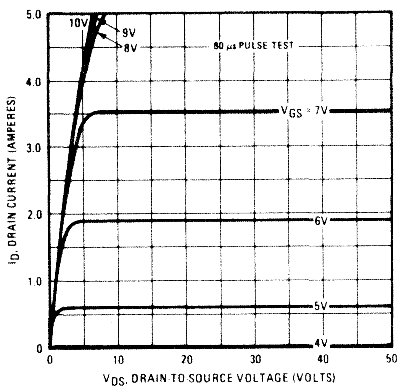


Fig. 2 — Typical Transfer Characteristics

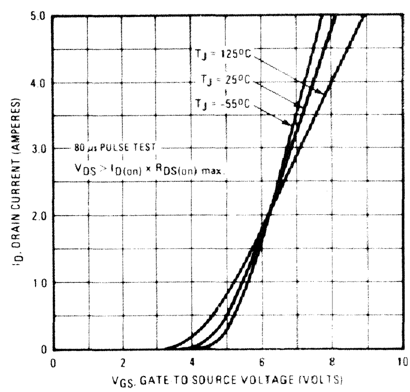


Fig. 3 — Typical Saturation Characteristics

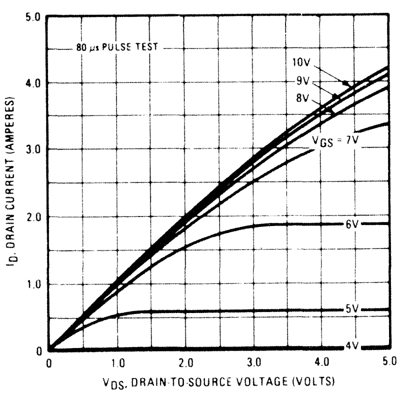


Fig. 4 — Maximum Safe Operating Area

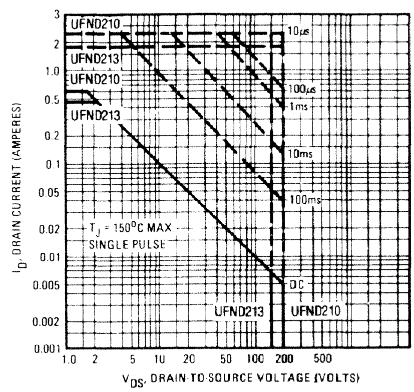


Fig. 5 — Typical Transconductance Vs. Drain Current

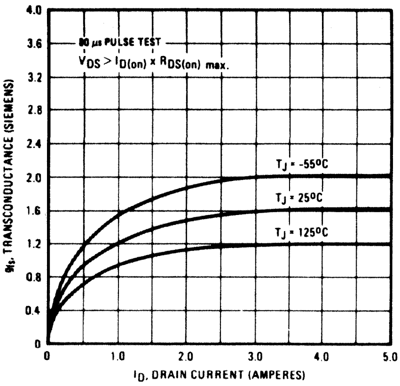


Fig. 6 — Typical Source-Drain Diode Forward Voltage

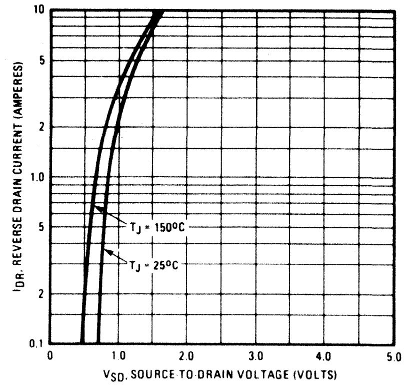


Fig. 7 — Breakdown Voltage Vs. Temperature

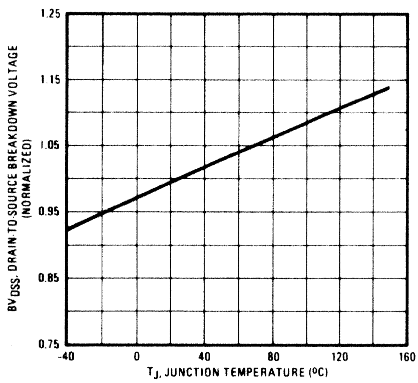


Fig. 8 — Normalized On-Resistance Vs. Temperature

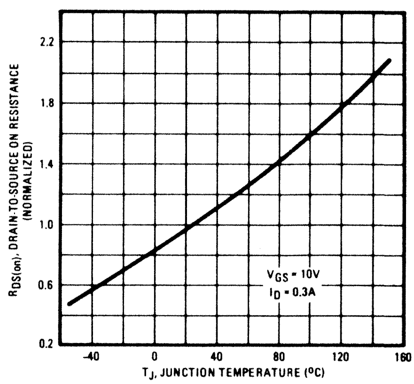


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Fig. 9 – Typical Capacitance Vs. Drain-to-Source Voltage

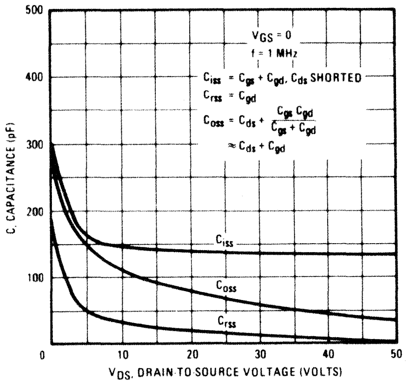


Fig. 10 – Typical Gate Charge Vs. Gate-to-Source Voltage

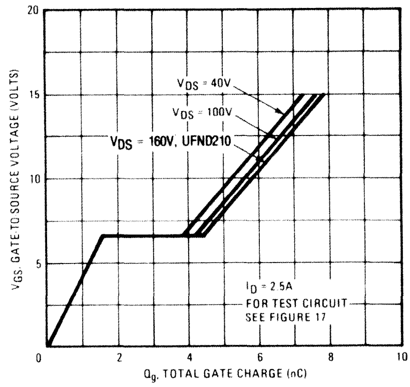


Fig. 11 – Typical On-Resistance Vs. Drain Current

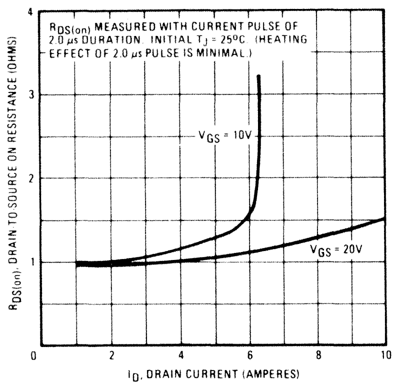


Fig. 12 – Maximum Drain Current Vs. Case Temperature

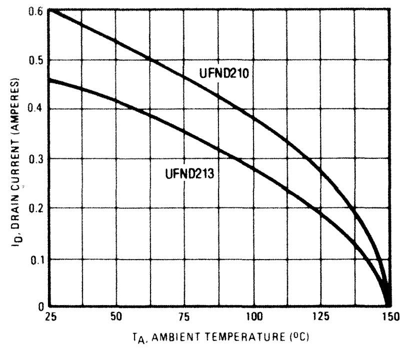


Fig. 13 – Power Vs. Temperature Derating Curve

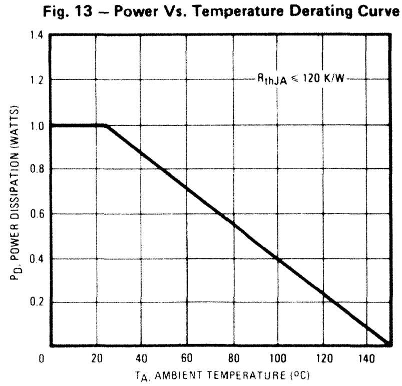


Fig. 14 — Clamped Inductive Test Circuit

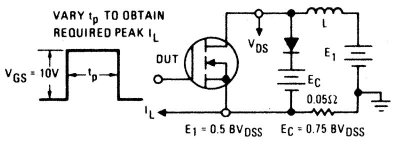


Fig. 15 — Clamped Inductive Waveforms

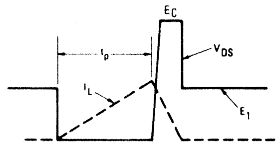


Fig. 16 — Switching Time Test Circuit

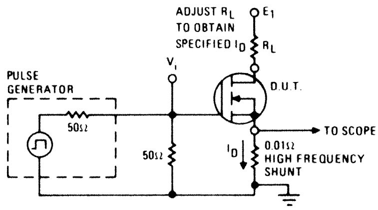
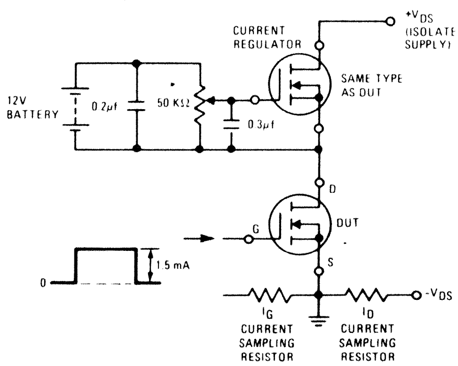


Fig. 17 — Gate Charge Test Circuit



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POWER MOSFET TRANSISTORS

100 Volt, 0.60 Ohm
N-Channel

UFNF110
UFNF111
UFNF112
UFNF113

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

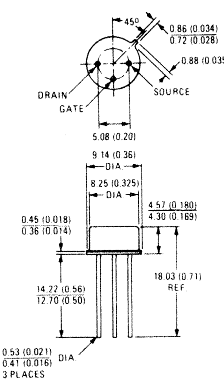
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFNF110	100V	0.6Ω	3.5A
UFNF111	60V	0.6Ω	3.5A
UFNF112	100V	0.8Ω	3.0A
UFNF113	60V	0.8Ω	3.0A

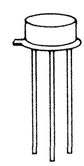
MECHANICAL SPECIFICATIONS

UFNF110 UFNF111 UFNF112 UFNF113



All Dimensions in Millimeters and (Inches)

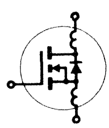
TO-39



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	UFNF110	UFNF111	UFNF112	UFNF113	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	3.5	3.5	3.0	3.0	A
I_{DM}	Pulsed Drain Current ③	14	14	12	12	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	15 (See Fig. 14)				W
	Linear Derating Factor	0.12 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 14	14	12	12	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

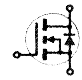
ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Symbol	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFNF110 UFNF112	100	—	—	V	V_{GS} = 0V
		UFNF111 UFNF113	60	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	−100	nA	V_{GS} = −20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFNF110 UFNF111	3.5	—	—	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		UFNF112 UFNF113	3.0	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFNF110 UFNF111	—	0.5	0.6	Ω	V_{GS} = 10V, I_D = 1.5A
		UFNF112 UFNF113	—	0.6	0.8	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	1.5	—	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 1.5A
C_{iss}	Input Capacitance	ALL	—	135	200	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	80	100	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	20	25	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	10	20	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 1.5A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	15	25	ns	
t_f	Fall Time	ALL	—	10	20	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	5.0	7.5	nC	V_{GS} = 10V, I_D = 8.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	2.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	3.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5 mm (0.2 in.) from header to center of die. / Modified MOSFET symbol showing the internal device inductances. 
L_S	Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.

THERMAL RESISTANCE

Symbol	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
R_{thJC}	Junction-to-Case	ALL	—	—	8.33	K/W	
R_{thJA}	Junction-to-Ambient	ALL	—	—	175	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFNF110 UFNF111	–	–	3.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFNF112 UFNF113	–	–	3.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFNF110 UFNF111	–	–	14	A	
		UFNF112 UFNF113	–	–	12	A	
V_{SD}	Diode Forward Voltage ②	UFNF110 UFNF111	–	–	2.5	V	$T_C = 25°C, I_S = 3.5A, V_{GS} = 0V$
		UFNF112 UFNF113	–	–	2.0	V	$T_C = 25°C, I_S = 3.0A, V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	–	200	–	ns	$T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	–	1.0	–	μC	$T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25°C$ to $150°C$. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

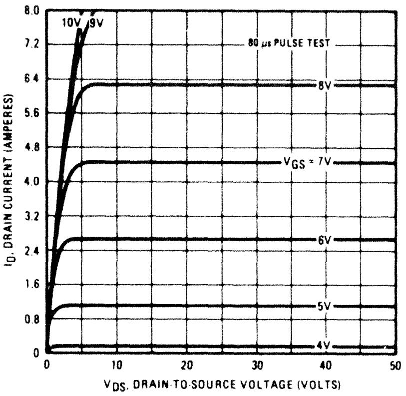


Fig. 2 — Typical Transfer Characteristics

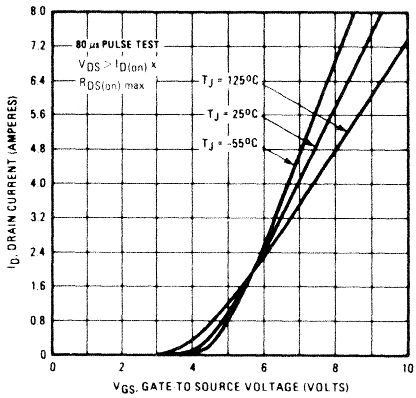


Fig. 3 — Typical Saturation Characteristics

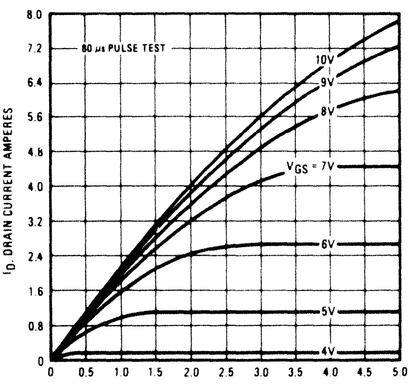


Fig. 4 — Maximum Safe Operating Area

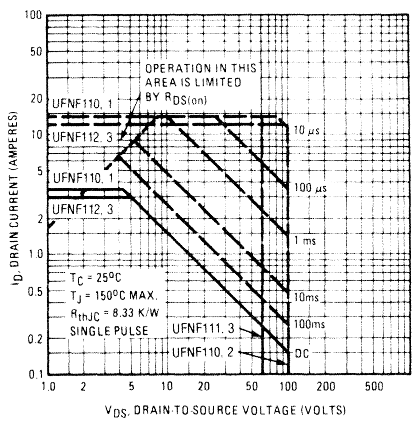


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

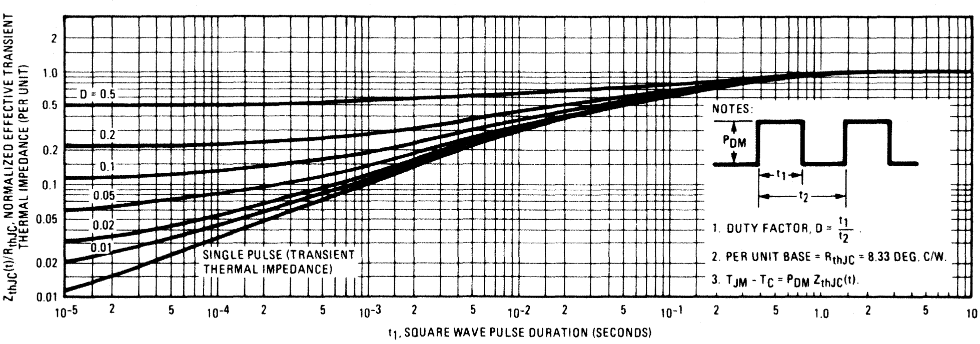


Fig. 6 — Typical Transconductance Vs. Drain Current

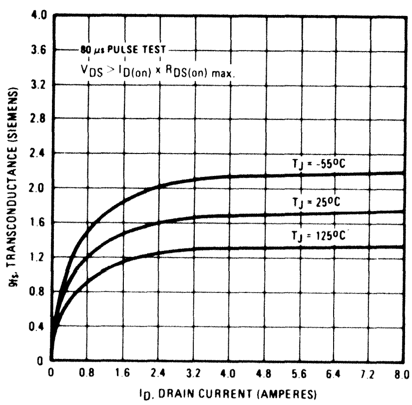


Fig. 7 — Typical Source-Drain Diode Forward Voltage

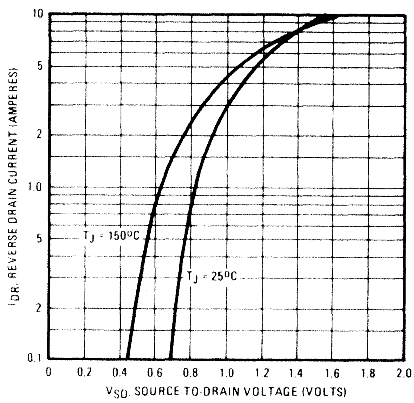


Fig. 8 — Breakdown Voltage Vs. Temperature

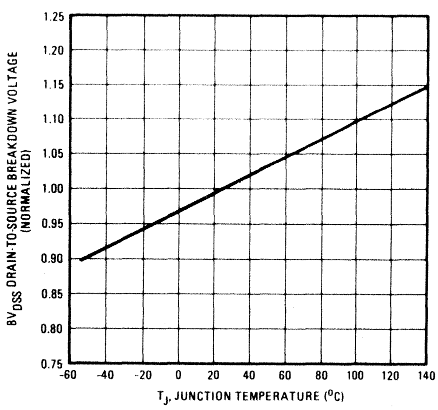


Fig. 9 — Normalized On-Resistance Vs. Temperature

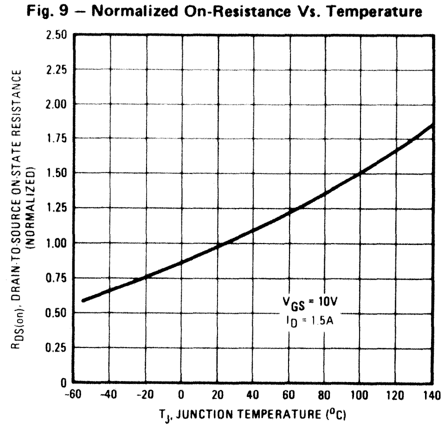


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

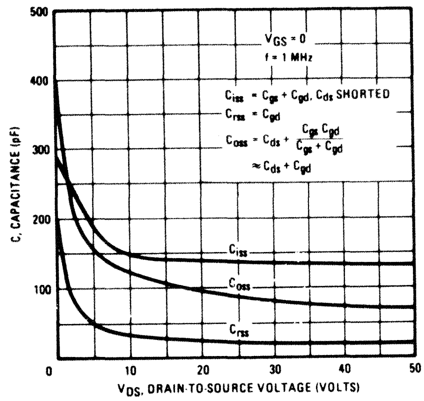


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

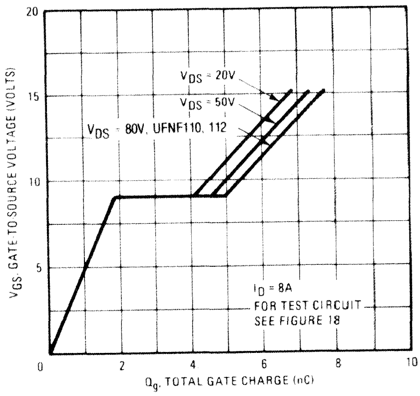


Fig. 12 — Typical On-Resistance Vs. Drain Current

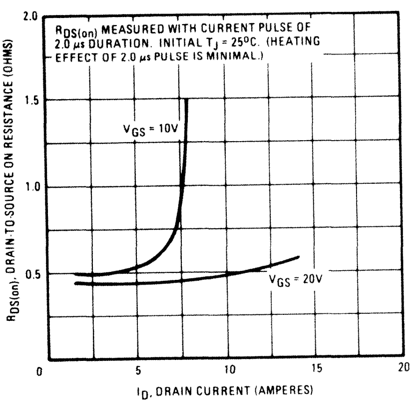


Fig. 13 — Maximum Drain Current Vs. Case Temperature

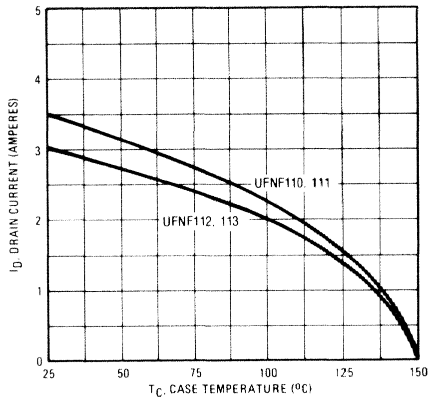


Fig. 14 — Power Vs. Temperature Derating Curve

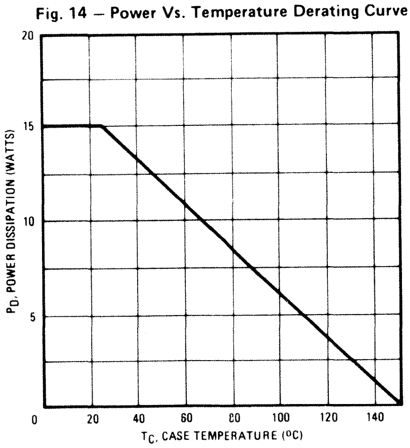


Fig. 15 — Clamped Inductive Test Circuit

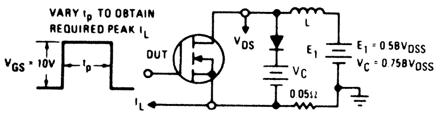


Fig. 16 — Clamped Inductive Waveforms

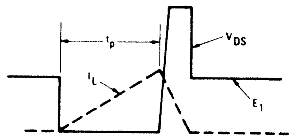


Fig. 17 — Switching Time Test Circuit

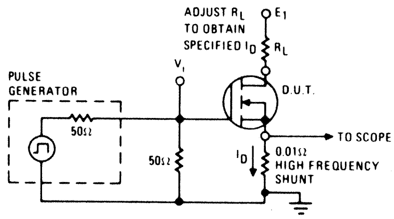
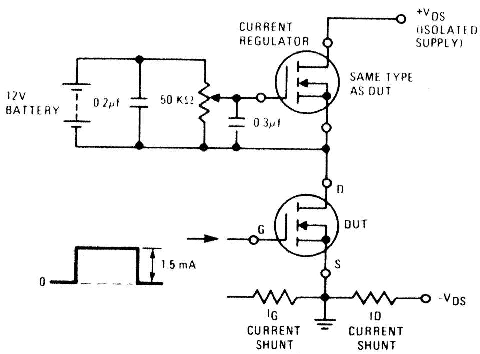


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

100 Volt, 0.30 Ohm
N-Channel

UFNF120
UFNF121
UFNF122
UFNF123

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

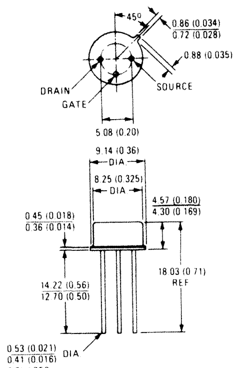
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFNF120	100V	0.30Ω	6.0A
UFNF121	60V	0.30Ω	6.0A
UFNF122	100V	0.40Ω	5.0A
UFNF123	60V	0.40Ω	5.0A

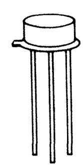
MECHANICAL SPECIFICATIONS

UFNF120 UFNF121 UFNF122 UFNF123



All Dimensions in Millimeters and (Inches)

TO-39



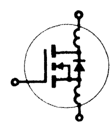
UNITRODE

ABSOLUTE MAXIMUM RATINGS

	Parameter	UFNF120	UFNF121	UFNF122	UFNF123	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	6.0	6.0	5.0	5.0	A
I_{DM}	Pulsed Drain Current ③	24	24	20	20	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped (See Fig. 15 and 16) L = 100μH	24	24	20	20	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

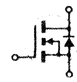
	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFNF120 UFNF122	100	–	–	V	V_{GS} = 0V
		UFNF121 UFNF123	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFNF120 UFNF121	6.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		UFNF122 UFNF123	5.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFNF120 UFNF121	–	0.25	0.30	Ω	V_{GS} = 10V, I_D = 3.0A
		UFNF122 UFNF123	–	0.30	0.40	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.5	2.9	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 3.0A
C_{iss}	Input Capacitance	ALL	–	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	200	400	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	50	100	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 3.0A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	37	70	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	35	70	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	10	15	nC	V_{GS} = 10V, I_D = 10A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	6.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	4.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 5 mm (0.2 in.) from header to center of die. / Modified MOSFET symbol showing the internal device inductances.
L_S	Internal Source Inductance	ALL	–	15	–	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.



THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	6.25	K/W	
R_{thJA}	Junction-to-Ambient	ALL	–	–	175	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFNF120 UFNF121	—	—	6.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFNF122 UFNF123	—	—	5.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFNF120 UFNF121	—	—	24	A	
		UFNF122 UFNF123	—	—	20	A	
V_{SD}	Diode Forward Voltage ②	UFNF120 UFNF121	—	—	2.5	V	$T_C = 25°C, I_S = 6.0A, V_{GS} = 0V$
		UFNF122 UFNF123	—	—	2.3	V	$T_C = 25°C, I_S = 5.0A, V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL		230		ns	$T_J = 150°C, I_F = 6.0A, dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	1.2	—	μC	$T_J = 150°C, I_F = 6.0A, dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

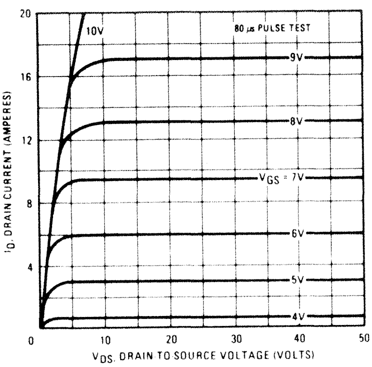


Fig. 2 — Typical Transfer Characteristics

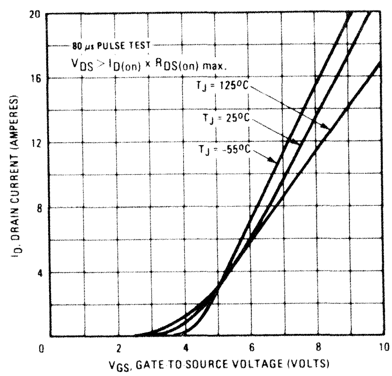


Fig. 3 — Typical Saturation Characteristics

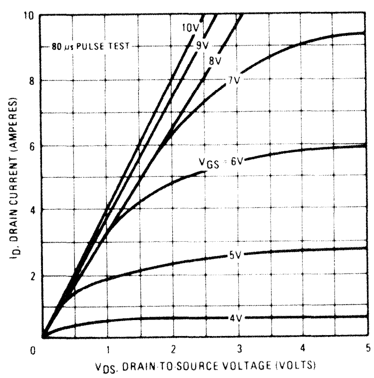


Fig. 4 — Maximum Safe Operating Area

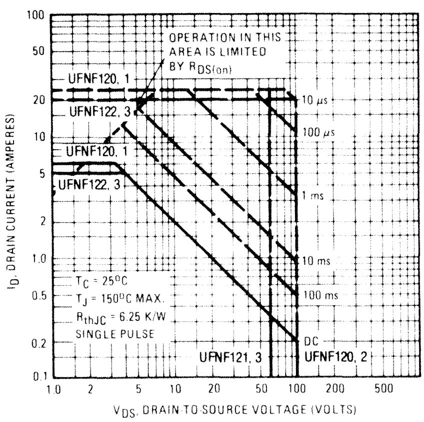


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

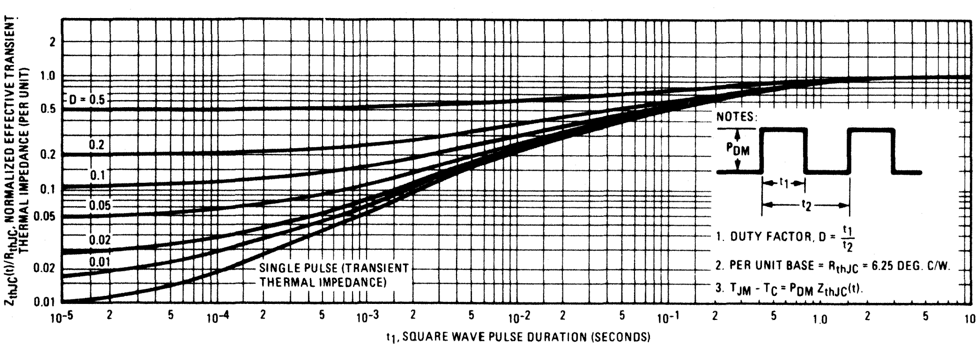


Fig. 6 — Typical Transconductance Vs. Drain Current

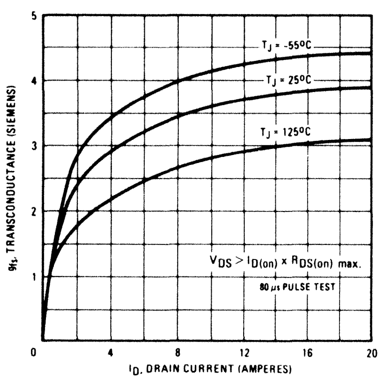


Fig. 7 — Typical Source-Drain Diode Forward Voltage

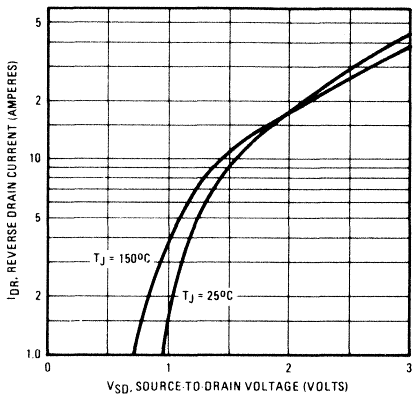


Fig. 8 — Breakdown Voltage Vs. Temperature

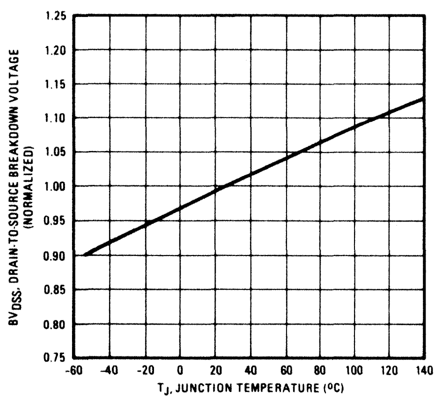


Fig. 9 — Normalized On-Resistance Vs. Temperature

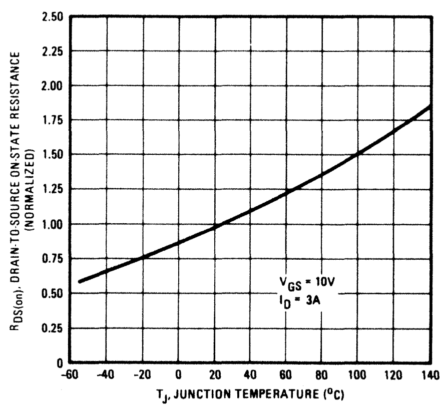


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

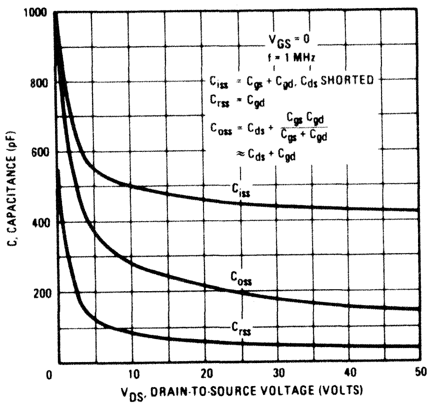


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

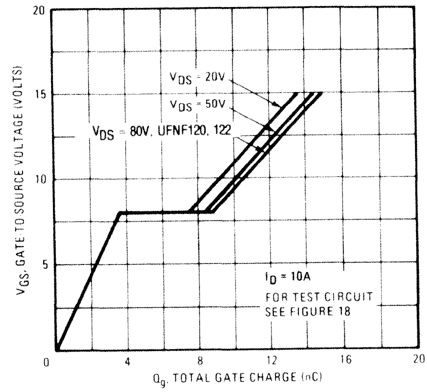


Fig. 12 — Typical On-Resistance Vs. Drain Current

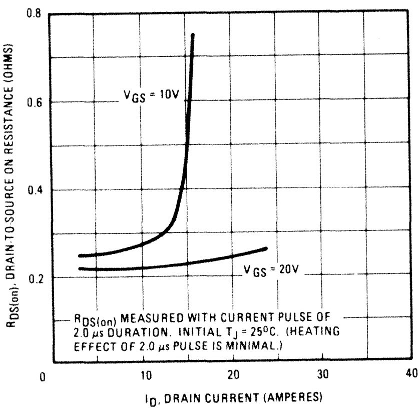


Fig. 13 — Maximum Drain Current Vs. Case Temperature

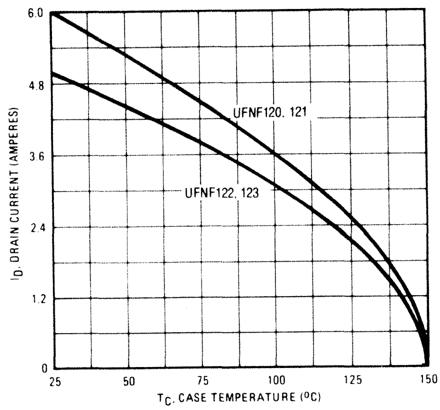


Fig. 14 — Power Vs. Temperature Derating Curve

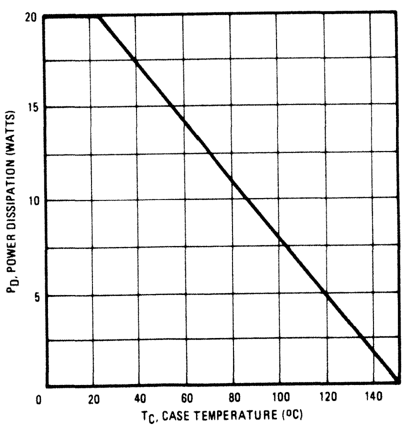


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Fig. 15 — Clamped Inductive Test Circuit

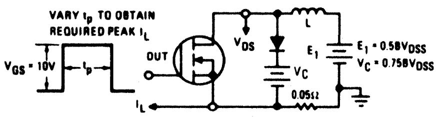


Fig. 16 — Clamped Inductive Waveforms

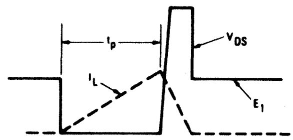


Fig. 17 — Switching Time Test Circuit

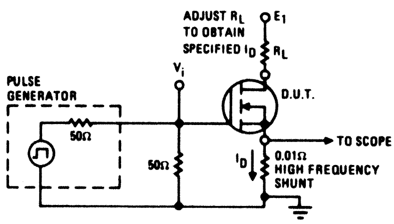
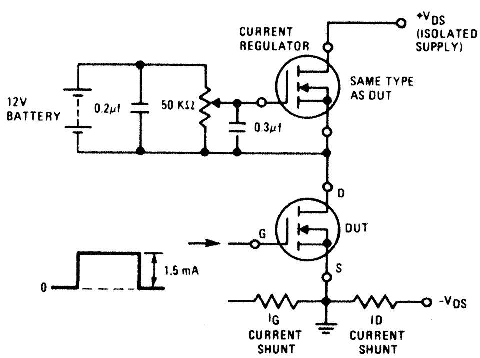


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

100 Volt, 0.18 Ohm
N-Channel

UFNF130
UFNF131
UFNF132
UFNF133

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

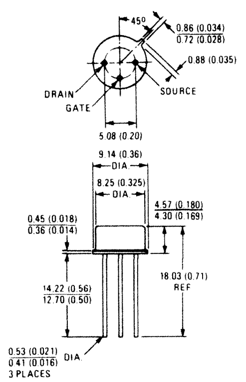
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFNF130	100V	0.18Ω	8.0A
UFNF131	60V	0.18Ω	8.0A
UFNF132	100V	0.25Ω	7.0A
UFNF133	60V	0.25Ω	7.0A

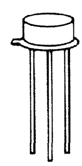
MECHANICAL SPECIFICATIONS

UFNF130 UFNF131 UFNF132 UFNF133



All Dimensions in Millimeters and (Inches)

TO-39

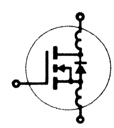


UNITRODE

ABSOLUTE MAXIMUM RATINGS

	Parameter	UFNF130	UFNF131	UFNF132	UFNF133	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_{DM}	Pulsed Drain Current ③	32	32	28	28	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	25 (See Fig. 14)				W
	Linear Derating Factor	0.2 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 32	32	28	28	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

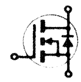
ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV_{DSS}	Drain - Source Breakdown Voltage	UFNF130 UFNF132	100	–	–	V	V_{GS} = 0V	
		UFNF131 UFNF133	60	–	–	V	I_D = 250μA	
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA	
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V	
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V	
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V	
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C	
$I_{D(on)}$	On-State Drain Current ②	UFNF130 UFNF131	8.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V	
		UFNF132 UFNF133	7.0	–	–	A		
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFNF130 UFNF131	–	0.14	0.18	Ω	V_{GS} = 10V, I_D = 4.0A	
		UFNF132 UFNF133	–	0.20	0.25	Ω		
g_{fs}	Forward Transconductance ②	ALL	4.0	5.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 4.0A	
C_{iss}	Input Capacitance	ALL	–	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10	
C_{oss}	Output Capacitance	ALL	–	300	500	pF		
C_{rss}	Reverse Transfer Capacitance	ALL	–	100	150	pF		
$t_{d(on)}$	Turn-On Delay Time	ALL	–	30	50	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 4.0A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t_r	Rise Time	ALL	–	80	150	ns		
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns		
t_f	Fall Time	ALL	–	80	150	ns		
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	18	30	nC	V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q_{gs}	Gate-Source Charge	ALL	–	9.0	–	nC		
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	9.0	–	nC		
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 5 mm (0.2 in.) from header to center of die.	Modified MOSFET symbol showing the internal device inductances.
L_S	Internal Source Inductance	ALL	–	15	–	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.	

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	5.0	K/W	
R_{thJA}	Junction-to-Ambient	ALL	–	–	175	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFNF130 UFNF131	—	—	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFNF132 UFNF133	—	—	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFNF130 UFNF131	—	—	32	A	
		UFNF132 UFNF133	—	—	28	A	
V_{SD}	Diode Forward Voltage ②	UFNF130 UFNF131	—	—	2.5	V	$T_C = 25°C, I_S = 8.0A, V_{GS} = 0V$
		UFNF132 UFNF133	—	—	2.3	V	$T_C = 25°C, I_S = 7.0A, V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	300	—	ns	$T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	1.5	—	μC	$T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

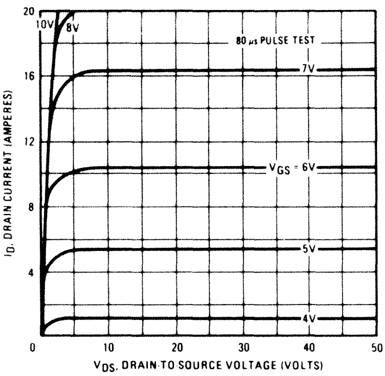


Fig. 2 — Typical Transfer Characteristics

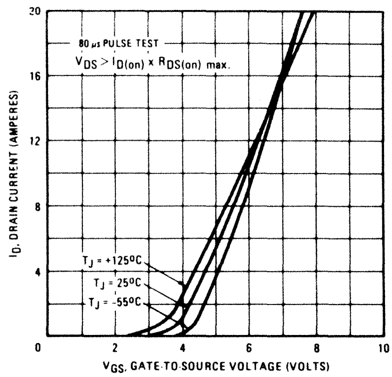


Fig. 3 — Typical Saturation Characteristics

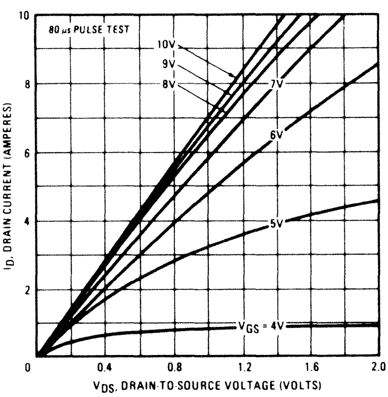


Fig. 4 — Maximum Safe Operating Area

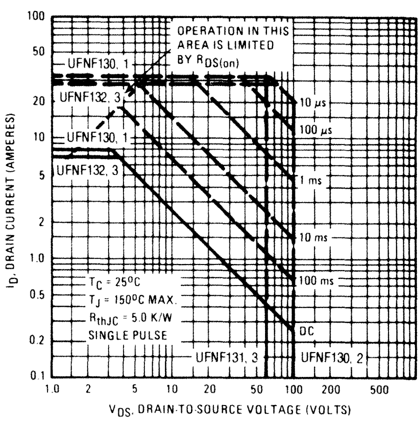


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

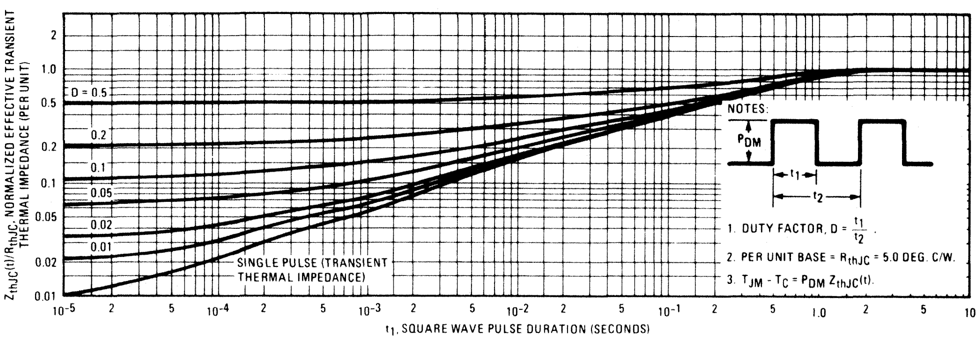


Fig. 6 — Typical Transconductance Vs. Drain Current

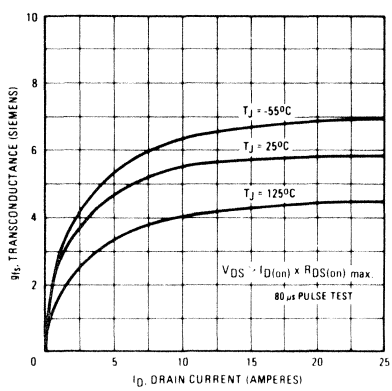


Fig. 7 — Typical Source-Drain Diode Forward Voltage

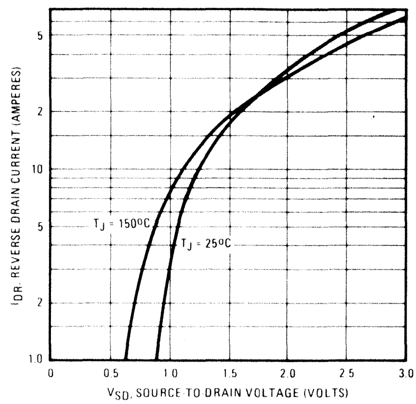


Fig. 8 — Breakdown Voltage Vs. Temperature

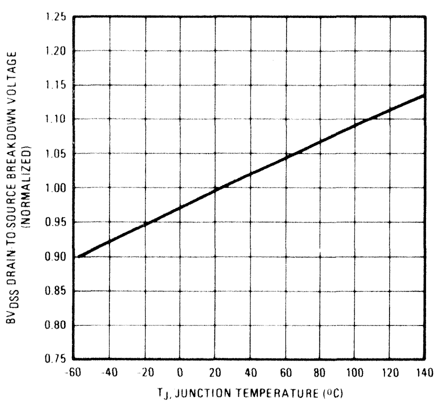


Fig. 9 — Normalized On-Resistance Vs. Temperature

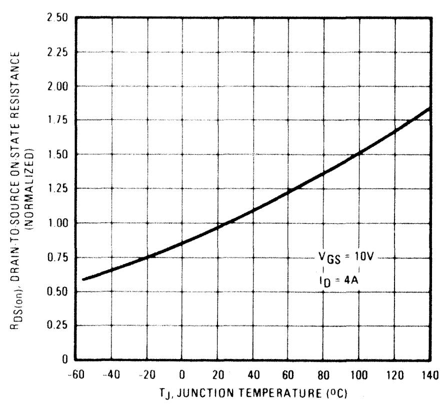


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Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

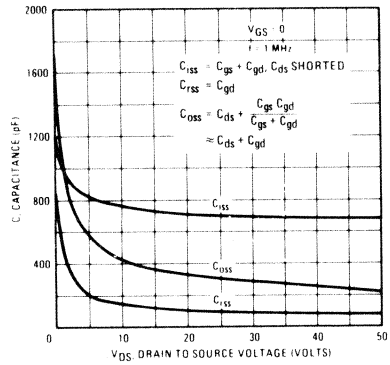


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

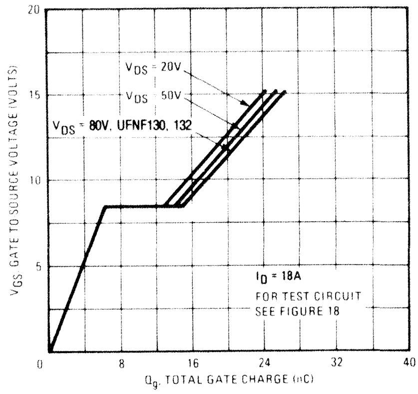


Fig. 12 – Typical On-Resistance Vs. Drain Current

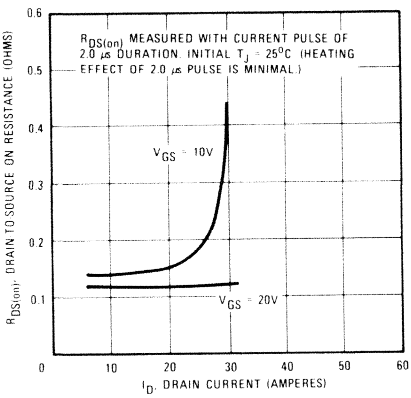


Fig. 13 – Maximum Drain Current Vs. Case Temperature

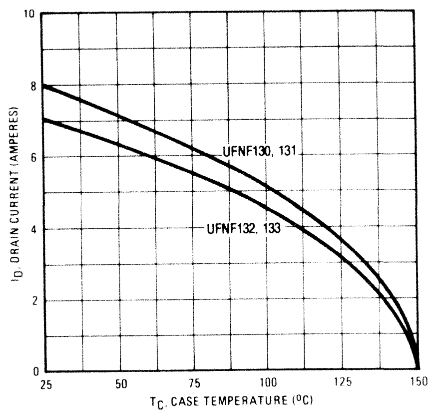


Fig. 14 – Power Vs. Temperature Derating Curve

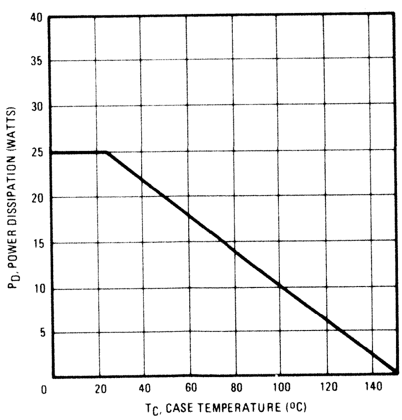


Fig. 15 – Clamped Inductive Test Circuit

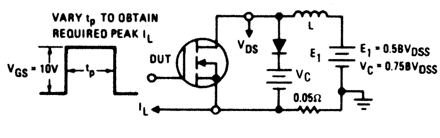


Fig. 16 – Clamped Inductive Waveforms

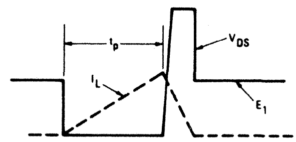


Fig. 17 – Switching Time Test Circuit

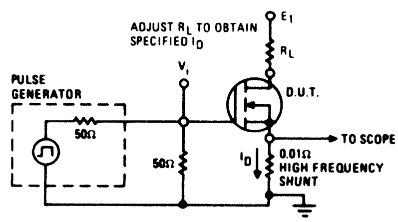
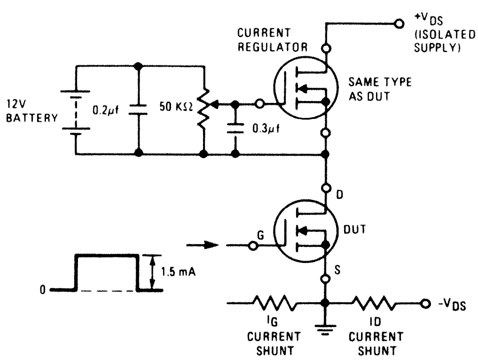


Fig. 18 – Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

200 Volt, 1.5 Ohm
N-Channel

UFNF210
UFNF211
UFNF212
UFNF213

FEATURES
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

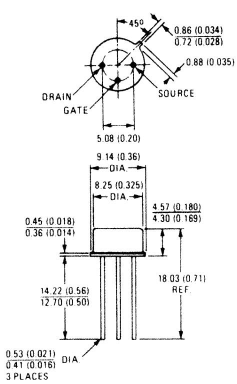
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFNF210	200V	1.5Ω	2.2A
UFNF211	150V	1.5Ω	2.2A
UFNF212	200V	2.4Ω	1.8A
UFNF213	150V	2.4Ω	1.8A

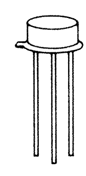
MECHANICAL SPECIFICATIONS

UFNF210 UFNF211 UFNF212 UFNF213



All Dimensions in Millimeters and (Inches)

TO-39

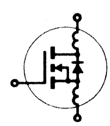


UNITRODE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	UFNF210	UFNF211	UFNF212	UFNF213	Units
V_{DS}	Drain — Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain — Gate Voltage (R_{GS} = 1 MΩ) ①	200	150	200	˙150	V
I_D @ T_C = 25°C	Continuous Drain Current	2.2	2.2	1.8	1.8	A
I_{DM}	Pulsed Drain Current ③	9.0	9.0	7.5	7.5	A
V_{GS}	Gate — Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	15 (See Fig. 14)				W
	Linear Derating Factor	0.12 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 9.0	9.0	7.5	7.5	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

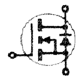
ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Symbol	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain — Source Breakdown Voltage	UFNF210 UFNF212	200	—	—	V	V_{GS} = 0V
		UFNF211 UFNF213	150	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate — Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate — Source Leakage Reverse	ALL	—	—	−100	nA	V_{GS} = −20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFNF210 UFNF211	2.2	—	—	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		UFNF212 UFNF213	1.8	—	—	A	
$R_{DS(on)}$	Static Drain — Source On-State Resistance ②	UFNF210 UFNF211	—	1.0	1.5	Ω	V_{GS} = 10V, I_D = 1.25A
		UFNF212 UFNF213	—	1.5	2.4	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.8	1.3	—	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 1.25A
C_{iss}	Input Capacitance	ALL	—	135	150	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	60	80	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	16	25	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	8.0	15	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 1.25A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	10	15	ns	
t_f	Fall Time	ALL	—	8.0	15	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	5.0	7.5	nC	V_{GS} = 10V, I_D = 4.5A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	2.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	3.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die. — Modified MOSFET symbol showing the internal device inductances. 
L_S	Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	—	—	8.33	K/W	
R_{thJA}	Junction-to-Ambient	ALL	—	—	175	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFNF210 UFNF211	—	—	2.2	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFNF212 UFNF213	—	—	1.8	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFNF210 UFNF211	—	—	9.0	A	
		UFNF212 UFNF213	—	—	7.5	A	
V_{SD}	Diode Forward Voltage ②	UFNF210 UFNF211	—	—	2.0	V	T_C = 25°C, I_S = 2.2A, V_{GS} = 0V
		UFNF212 UFNF213	—	—	1.8	V	T_C = 25°C, I_S = 1.8A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	290	—	ns	T_J = 150°C, I_F = 2.2A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	2.0	—	μC	T_J = 150°C, I_F = 2.2A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

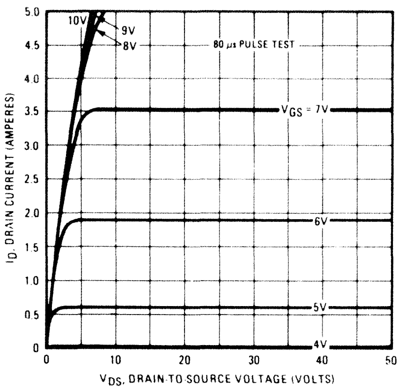


Fig. 2 — Typical Transfer Characteristics

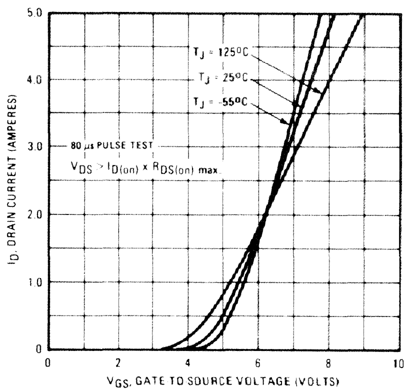


Fig. 3 — Typical Saturation Characteristics

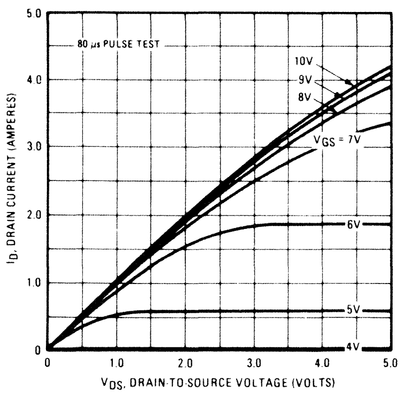


Fig. 4 — Maximum Safe Operating Area

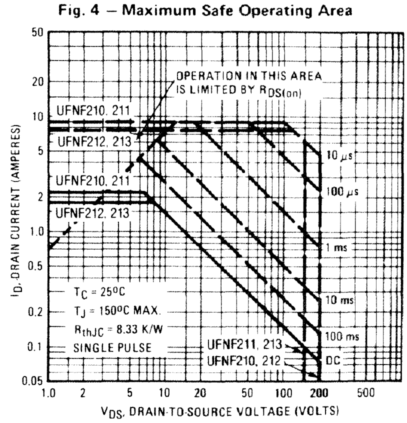


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

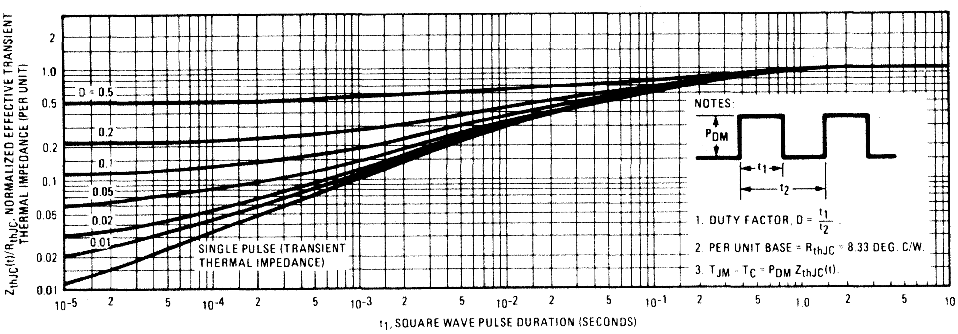


Fig. 6 — Typical Transconductance Vs. Drain Current

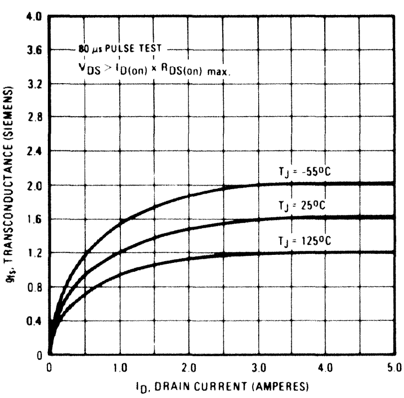


Fig. 7 — Typical Source-Drain Diode Forward Voltage

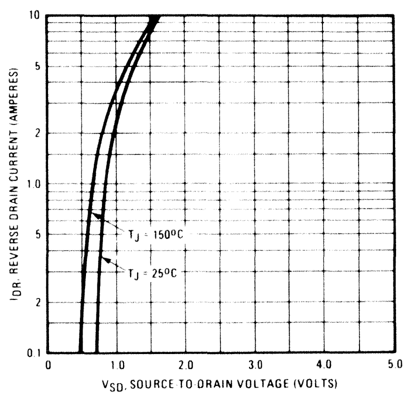


Fig. 8 — Breakdown Voltage Vs. Temperature

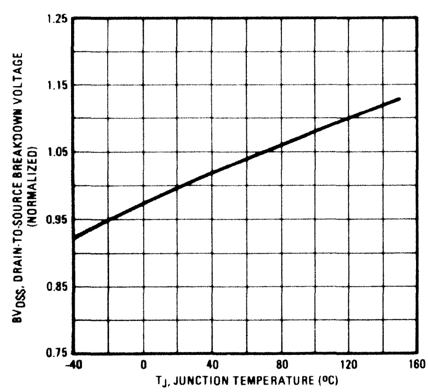


Fig. 9 — Normalized On-Resistance Vs. Temperature

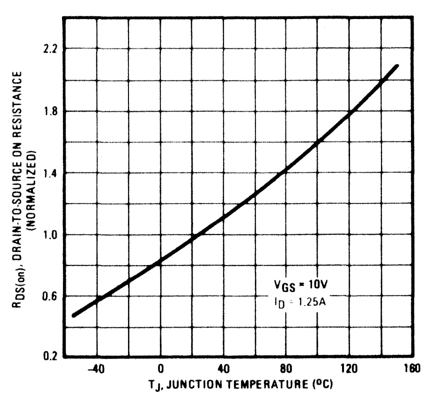


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

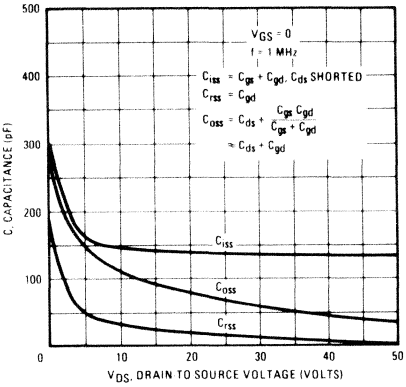


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

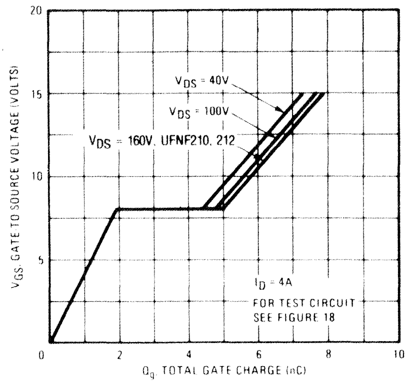


Fig. 12 — Typical On-Resistance Vs. Drain Current

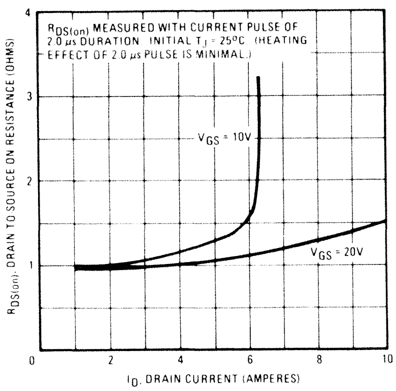


Fig. 13 — Maximum Drain Current Vs. Case Temperature

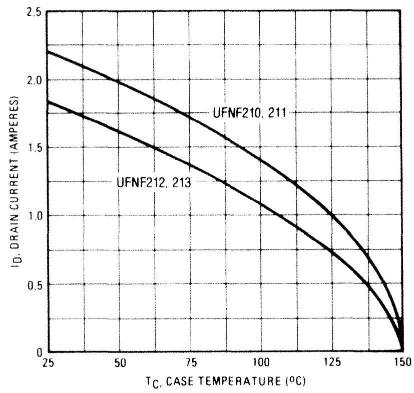


Fig. 14 — Power Vs. Temperature Derating Curve

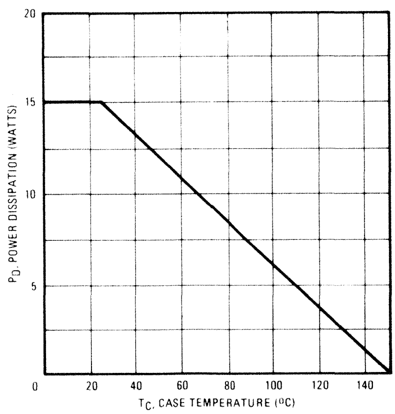


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Fig. 15 – Clamped Inductive Test Circuit

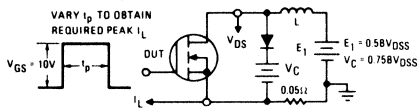


Fig. 16 – Clamped Inductive Waveforms

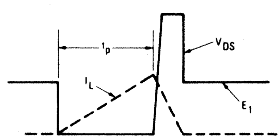


Fig. 17 – Switching Time Test Circuit

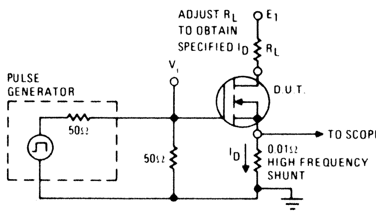
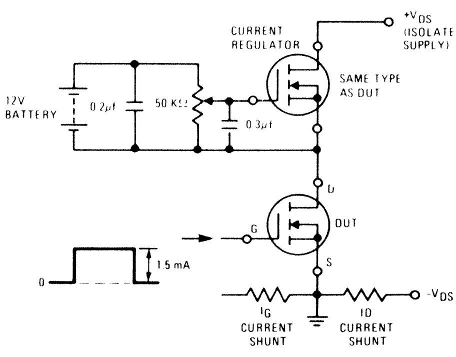


Fig. 18 – Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

200 Volt, 0.8 Ohm
N-Channel

UFNF220
UFNF221
UFNF222
UFNF223

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

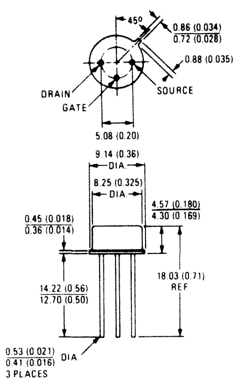
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFNF220	200V	0.8Ω	3.5A
UFNF221	150V	0.8Ω	3.5A
UFNF222	200V	1.2Ω	3.0A
UFNF223	150V	1.2Ω	3.0A

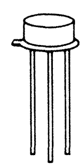
MECHANICAL SPECIFICATIONS

UFNF220 UFNF221 UFNF222 UFNF223



All Dimensions in Millimeters and (Inches)

TO-39



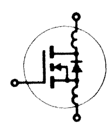
UNITRODE

ABSOLUTE MAXIMUM RATINGS

Parameter		UFNF220	UFNF221	UFNF222	UFNF223	Units
V_{DS}	Drain — Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain — Gate Voltage (R_{GS} = 1 MΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	3.5	3.5	3.0	3.0	A
I_{DM}	Pulsed Drain Current ③	14	14	12	12	A
V_{GS}	Gate — Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 14	14	12	12	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

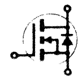
Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain — Source Breakdown Voltage	UFNF220 UFNF222	200	—	—	V	V_{GS} = 0V
		UFNF221 UFNF223	150	—		V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate — Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate — Source Leakage Reverse	ALL	—	—	−100	nA	V_{GS} = −20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFNF220 UFNF221	3.5	—	—	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		UFNF222 UFNF223	3.0	—	—	A	
$R_{DS(on)}$	Static Drain — Source On-State Resistance ②	UFNF220 UFNF221	—	0.5	0.8	Ω	V_{GS} = 10V, I_D = 2.0A
		UFNF222 UFNF223	—	0.8	1.2	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.5	2.25		S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 2.0A
C_{iss}	Input Capacitance	ALL	—	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	150	300	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	40	80	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	20	40	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 2.0A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	30	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	50	100	ns	
t_f	Fall Time	ALL	—	30	60	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL		11	15	nC	V_{GS} = 10V, I_D = 7.0A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	5.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	6.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die. / Modified MOSFET symbol showing the internal device inductances.
L_S	Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.



THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	—	—	6.25	K/W	
R_{thJA}	Junction-to-Ambient	ALL	—	—	175	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFNF220 UFNF221	—	—	3.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFNF222 UFNF223	—	—	3.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFNF220 UFNF221	—	—	14	A	
		UFNF222 UFNF223	—	—	12	A	
V_{SD}	Diode Forward Voltage ②	UFNF220 UFNF221	—	—	2.0	V	$T_C = 25°C, I_S = 3.5A, V_{GS} = 0V$
		UFNF222 UFNF223	—	—	1.8	V	$T_C = 25°C, I_S = 3.0A, V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	350	—	ns	$T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	2.3	—	μC	$T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

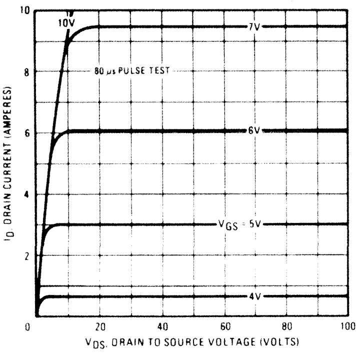


Fig. 2 — Typical Transfer Characteristics

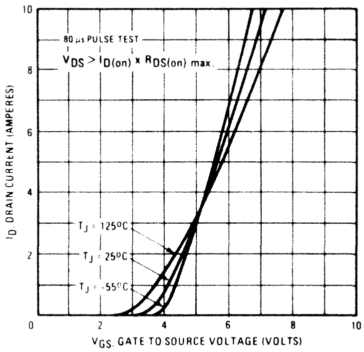


Fig. 3 — Typical Saturation Characteristics

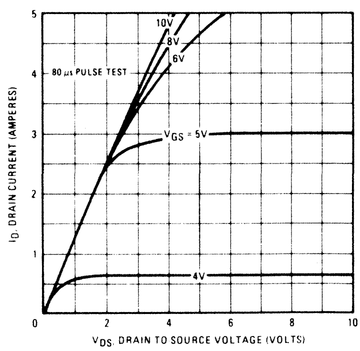


Fig. 4 — Maximum Safe Operating Area

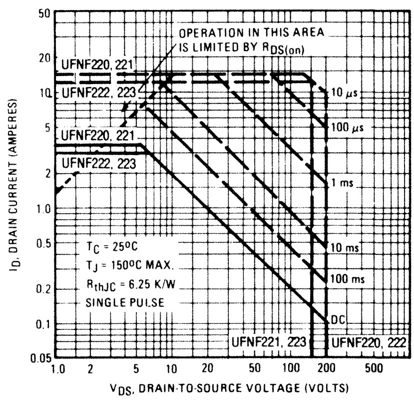


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Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

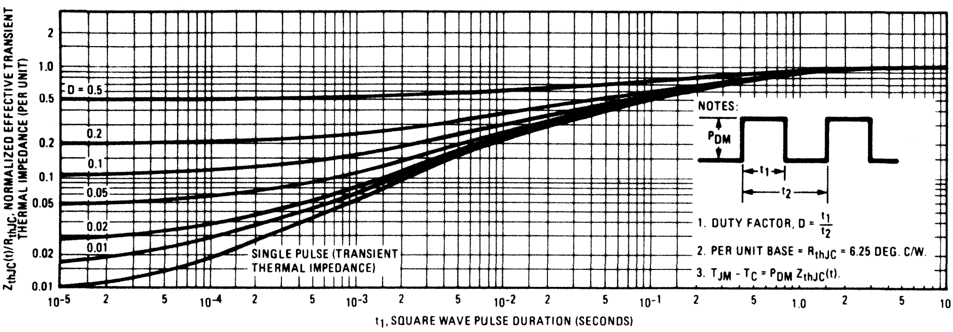

Fig. 6 — Typical Transconductance Vs. Drain Current

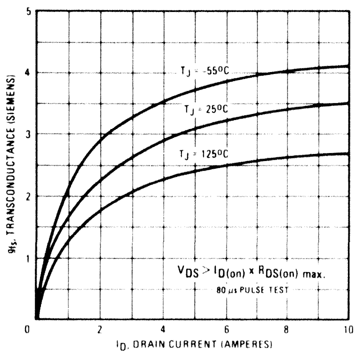

Fig. 7 — Typical Source-Drain Diode Forward Voltage

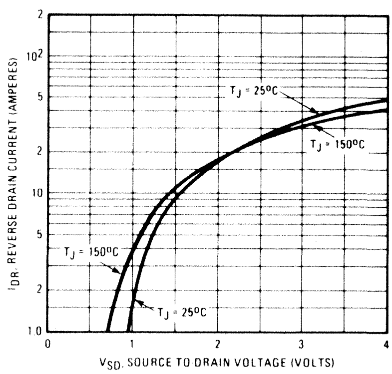

Fig. 8 — Breakdown Voltage Vs. Temperature

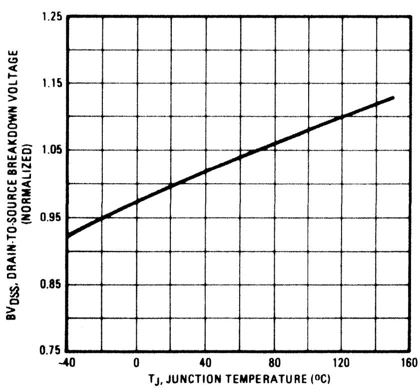

Fig. 9 — Normalized On-Resistance Vs. Temperature

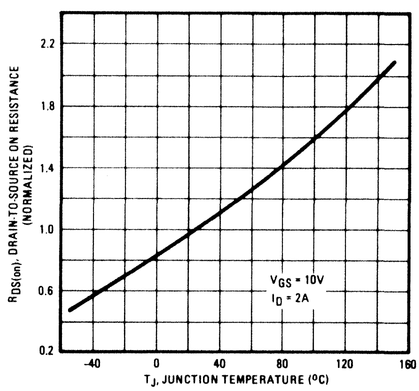

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Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

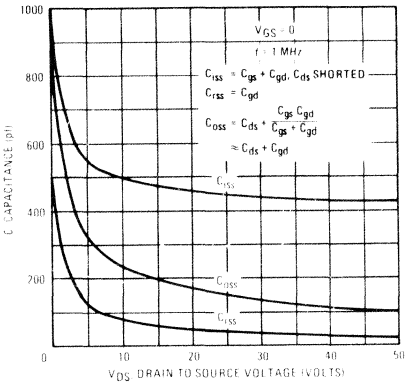


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

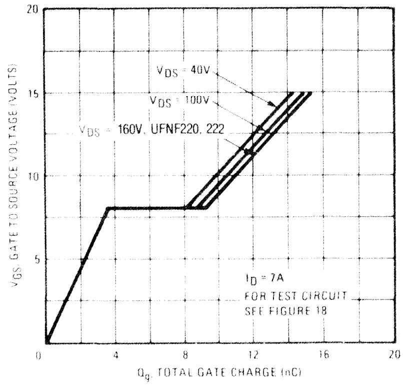


Fig. 12 – Typical On-Resistance Vs. Drain Current

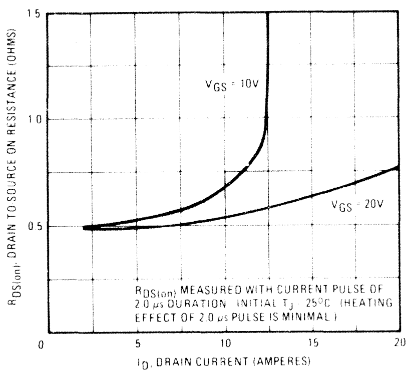


Fig. 13 – Maximum Drain Current Vs. Case Temperature

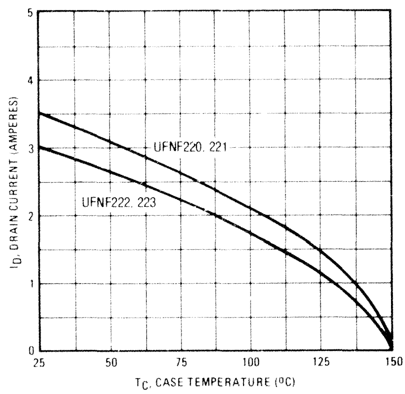


Fig. 14 – Power Vs. Temperature Derating Curve

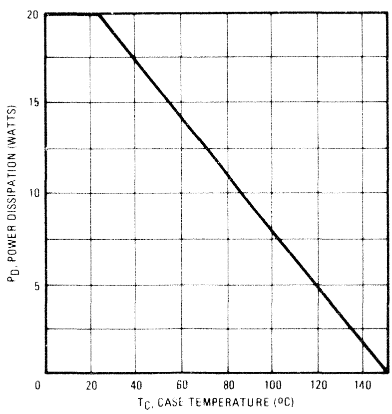


Fig. 15 – Clamped Inductive Test Circuit

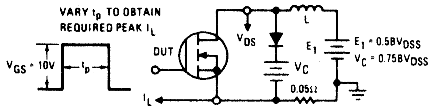


Fig. 16 – Clamped Inductive Waveforms

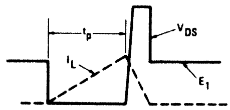


Fig. 17 – Switching Time Test Circuit

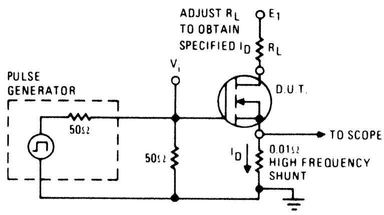
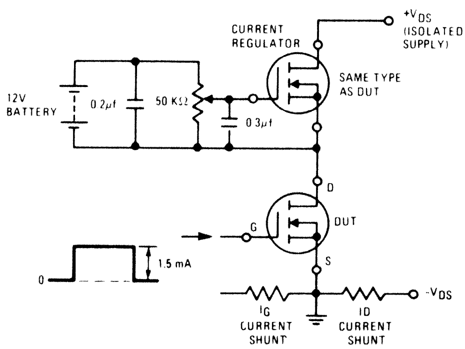


Fig. 18 – Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

200 Volt, 0.4 Ohm
N-Channel

UFNF230
UFNF231
UFNF232
UFNF233

FEATURES
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

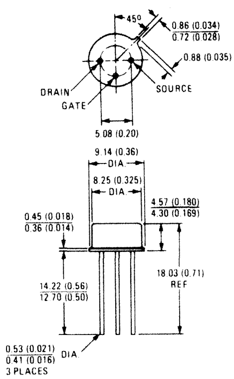
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFNF230	200V	0.4Ω	5.5A
UFNF231	150V	0.4Ω	5.5A
UFNF232	200V	0.6Ω	4.5A
UFNF233	150V	0.6Ω	4.5A

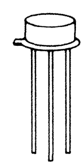
MECHANICAL SPECIFICATIONS

UFNF230 UFNF231 UFNF232 UFNF233



All Dimensions in Millimeters and (Inches)

TO-39



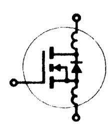
UNITRODE

ABSOLUTE MAXIMUM RATINGS

	Parameter	UFNF230	UFNF231	UFNF232	UFNF233	Units
V_{DS}	Drain — Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain — Gate Voltage (R_{GS} = 1 MΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	5.5	5.5	4.5	4.5	A
I_{DM}	Pulsed Drain Current ③	22	22	18	18	A
V_{GS}	Gate — Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	25 (See Fig. 14)				W
	Linear Derating Factor	0.2 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 22	22	18	18	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

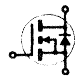
	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain — Source Breakdown Voltage	UFNF230 UFNF232	200	—	—	V	V_{GS} = 0V
		UFNF231 UFNF233	150	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate — Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate — Source Leakage Reverse	ALL	—	—	−100	nA	V_{GS} = −20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFNF230 UFNF231	5.5	—	—	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		UFNF232 UFNF233	4.5	—	—	A	
$R_{DS(on)}$	Static Drain — Source On-State Resistance ②	UFNF230 UFNF231	—	0.25	0.4	Ω	V_{GS} = 10V, I_D = 3.0A
		UFNF232 UFNF233	—	0.4	0.6	Ω	
g_{fs}	Forward Transconductance ②	ALL	2.5	4.5	—	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 3.0A
C_{iss}	Input Capacitance	ALL	—	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	250	450	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	80	150	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	—	30	ns	V_{DD} = 90V, I_D = 3.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	—	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	—	50	ns	
t_f	Fall Time	ALL	—	—	40	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL		19	30	nC	V_{GS} = 10V, I_D = 11A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	10	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	9.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die. — Modified MOSFET symbol showing the internal device inductances.
L_S	Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.



THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	—	—	5.0	K/W	
R_{thJA}	Junction-to-Ambient	ALL	—	—	175	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFNF230 UFNF231	—	—	5.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFNF232 UFNF233	—	—	4.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFNF230 UFNF231	—	—	22	A	
		UFNF232 UFNF233	—	—	18	A	
V_{SD}	Diode Forward Voltage ②	UFNF230 UFNF231	—	—	2.0	V	$T_C = 25°C, I_S = 5.5A, V_{GS} = 0V$
		UFNF232 UFNF233	—	—	1.8	V	$T_C = 25°C, I_S = 4.5A, V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	450	—	ns	$T_J = 150°C, I_F = 5.5A, dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	3.0	—	μC	$T_J = 150°C, I_F = 5.5A, dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

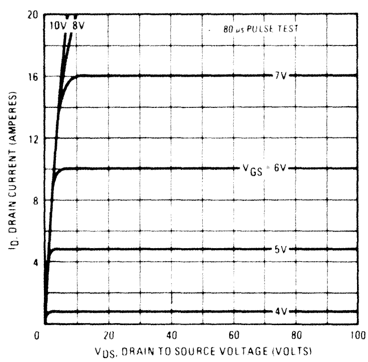


Fig. 2 — Typical Transfer Characteristics

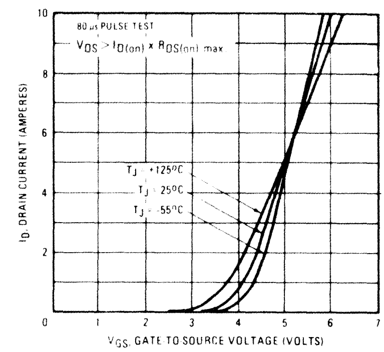


Fig. 3 — Typical Saturation Characteristics

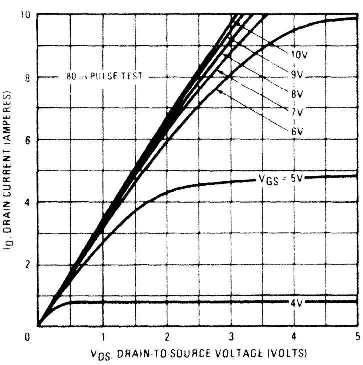


Fig. 4 — Maximum Safe Operating Area

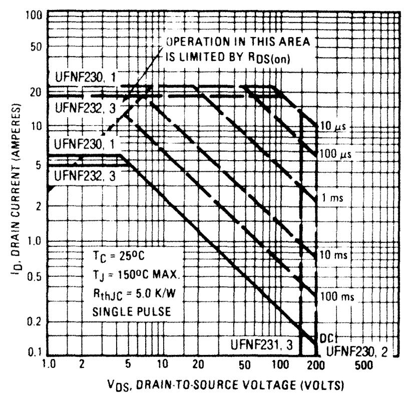


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

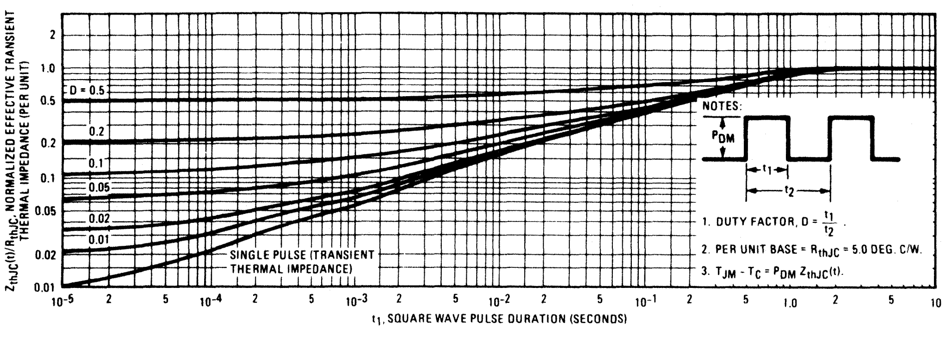


Fig. 6 — Typical Transconductance Vs. Drain Current

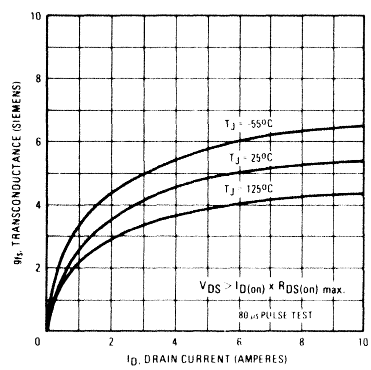


Fig. 7 — Typical Source-Drain Diode Forward Voltage

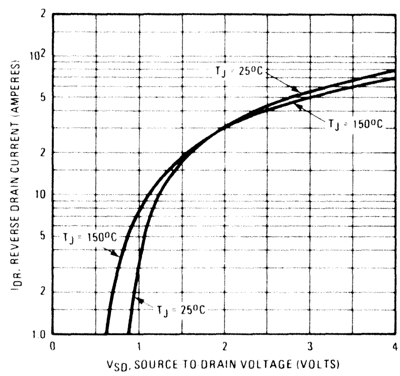


Fig. 8 — Breakdown Voltage Vs. Temperature

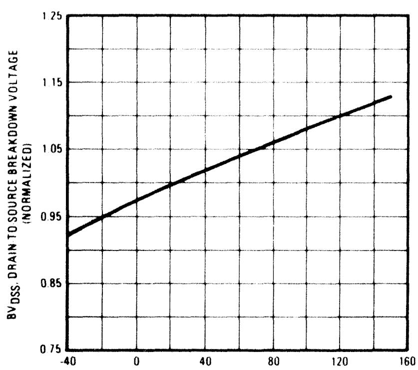


Fig. 9 — Normalized On-Resistance Vs. Temperature

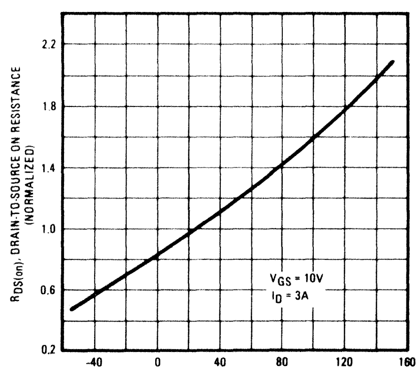


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

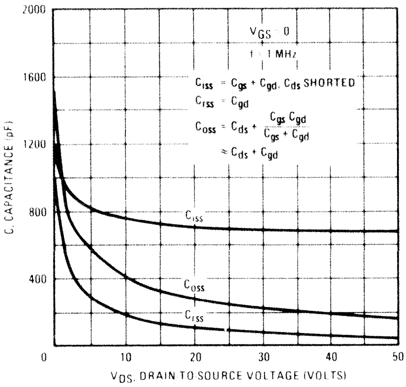


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

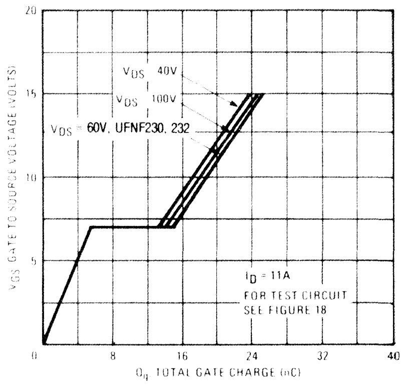


Fig. 12 – Typical On-Resistance Vs. Drain Current

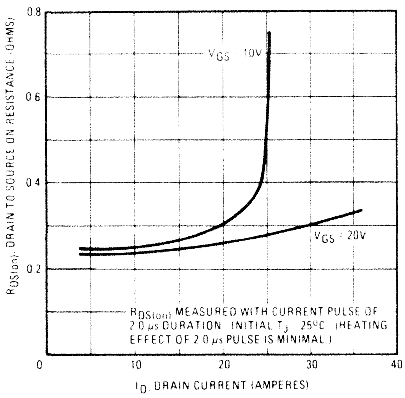


Fig. 13 – Maximum Drain Current Vs. Case Temperature

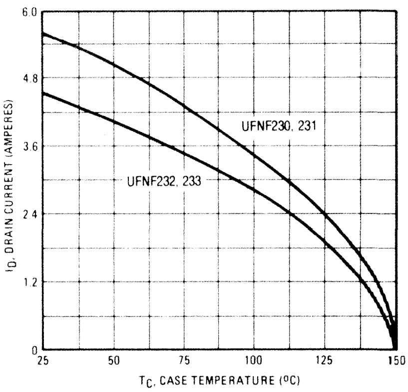


Fig. 14 – Power Vs. Temperature Derating Curve

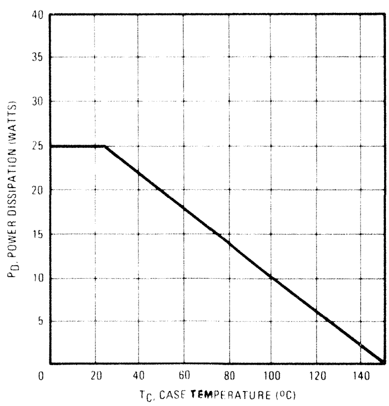


Fig. 15 — Clamped Inductive Test Circuit

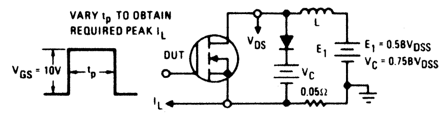


Fig. 16 — Clamped Inductive Waveforms

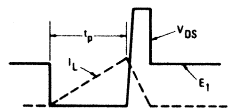


Fig. 17 — Switching Time Test Circuit

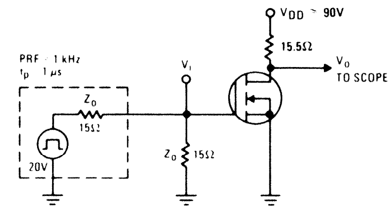
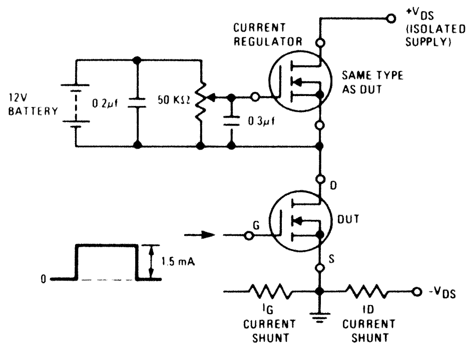


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS
500 Volt, 1.5 Ohm
N-Channel

UFNF430
UFNF431
UFNF432
UFNF433

FEATURES
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

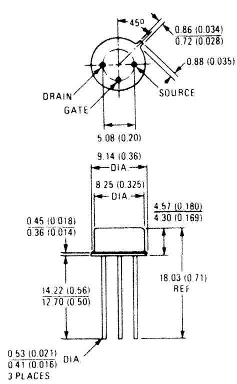
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFNF430	500V	1.5Ω	2.75A
UFNF431	450V	1.5Ω	2.75A
UFNF432	500V	2.0Ω	2.25A
UFNF433	450V	2.0Ω	2.25A

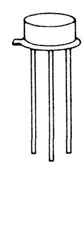
MECHANICAL SPECIFICATIONS

UFNF430 UFNF431 UFNF432 UFNF433



All Dimensions in Millimeters and (Inches)

TO-39



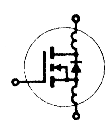
UNITRODE

ABSOLUTE MAXIMUM RATINGS

Parameter		UFNF430	UFNF431	UFNF432	UFNF433	Units
V_{DS}	Drain – Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 1 MΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	2.75	2.75	2.25	2.25	A
I_{DM}	Pulsed Drain Current ③	11	11	9.0	9.0	A
V_{GS}	Gate – Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	25 (See Fig. 14)				W
	Linear Derating Factor	0.2 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 11	11	9.0	9.0	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

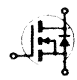
Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	UFNF430 UFNF432	500	–	–	V	V_{GS} = 0V
		UFNF431 UFNF433	450	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate – Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate – Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFNF430 UFNF431	2.75	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		UFNF432 UFNF433	2.25	–	–	A	
$R_{DS(on)}$	Static Drain – Source On-State Resistance ②	UFNF430 UFNF431	–	1.3	1.5	Ω	V_{GS} = 10V, I_D = 1.5A
		UFNF432 UFNF433	–	1.5	2.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.5	2.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 1.5A
C_{iss}	Input Capacitance	ALL	–	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	100	200	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	30	60	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} = 225V, I_D = 1.5A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	30	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	55	ns	
t_f	Fall Time	ALL	–	–	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	22	30	nC	V_{GS} = 10V, I_D = 6.0A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	11	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	11	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die. — Modified MOSFET symbol showing the internal device inductances.
L_S	Internal Source Inductance	ALL	–	15	–	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.



THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	5.0	K/W	
R_{thJA}	Junction-to-Ambient	ALL	–	–	175	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFNF430 UFNF431	—		2.75	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFNF432 UFNF433	—	—	2.25	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFNF430 UFNF431	—		11	A	
		UFNF432 UFNF433	—	—	9.0	A	
V_{SD}	Diode Forward Voltage ②	UFNF430 UFNF431	—	—	1.4	V	T_C = 25°C, I_S = 2.75A, V_{GS} = 0V
		UFNF432 UFNF433	—		1.3	V	T_C = 25°C, I_S = 2.25A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	800	—	ns	T_J = 150°C, I_F = 2.75A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	4.6	—	μC	T_J = 150°C, I_F = 2.75A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

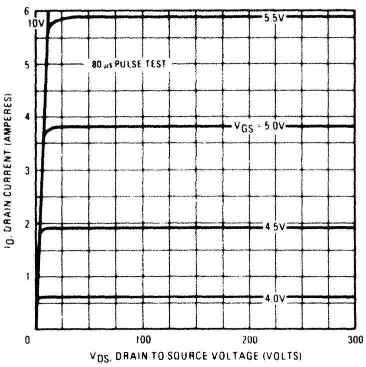


Fig. 2 — Typical Transfer Characteristics

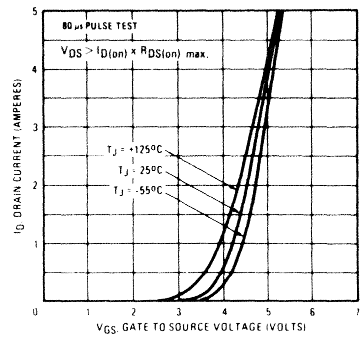


Fig. 3 — Typical Saturation Characteristics

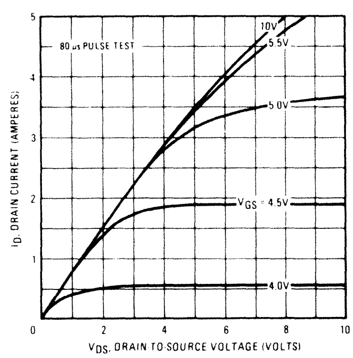


Fig. 4 — Maximum Safe Operating Area

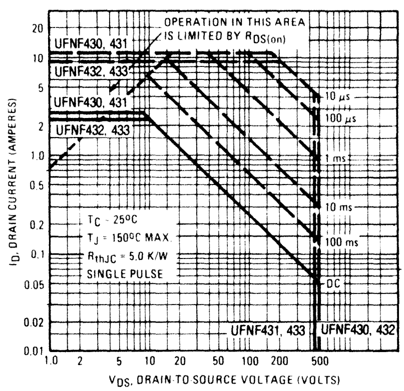


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

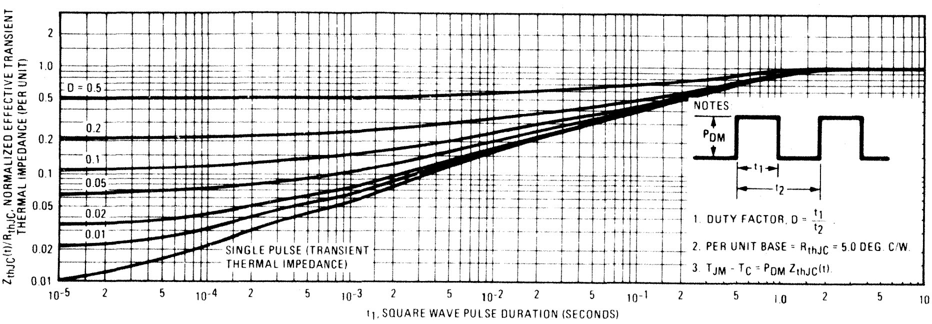


Fig. 6 — Typical Transconductance Vs. Drain Current

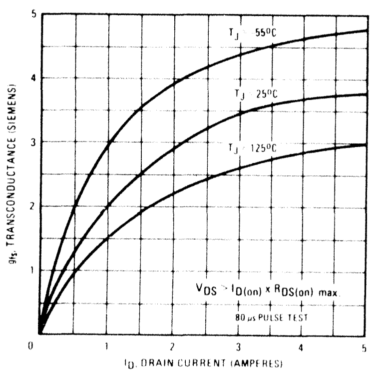


Fig. 7 — Typical Source-Drain Diode Forward Voltage

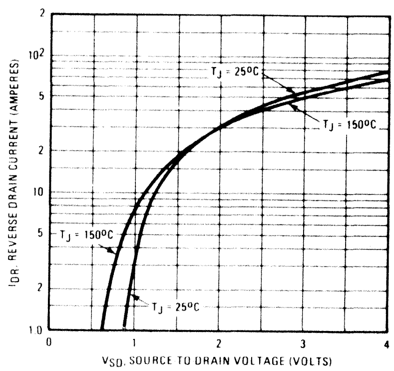


Fig. 8 — Breakdown Voltage Vs. Temperature

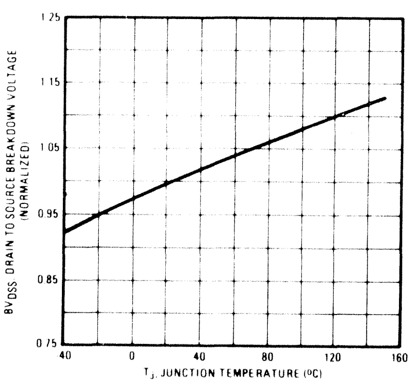


Fig. 9 — Normalized On-Resistance Vs. Temperature

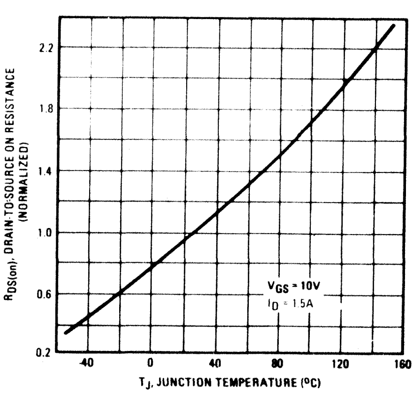


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

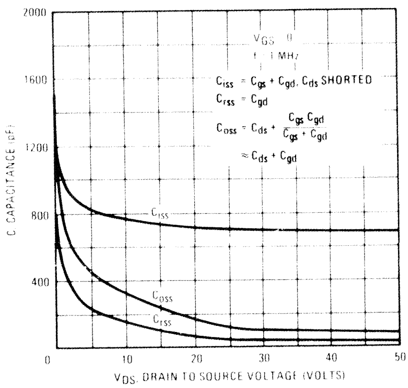


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

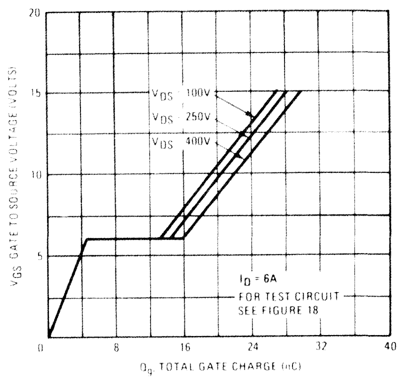


Fig. 12 — Typical On-Resistance Vs. Drain Current

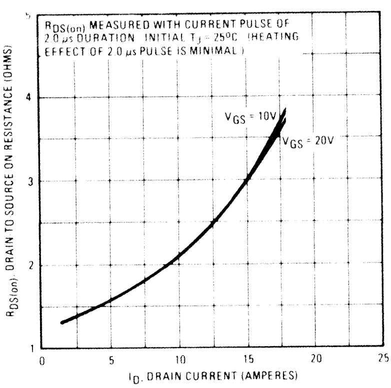


Fig. 13 — Maximum Drain Current Vs. Case Temperature

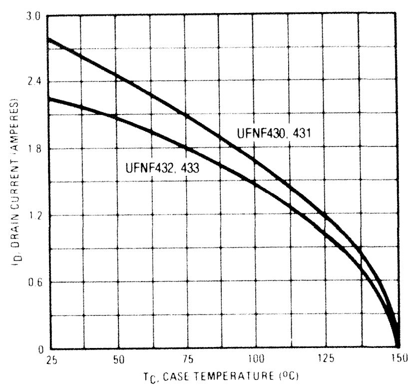


Fig. 14 — Power Vs. Temperature Derating Curve

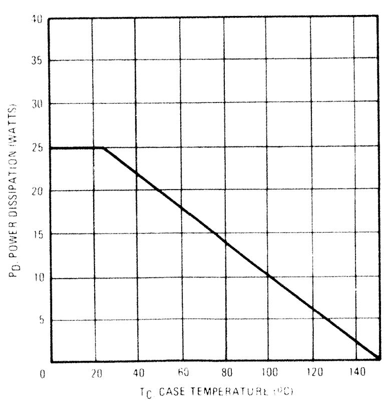


Fig. 15 — Clamped Inductive Test Circuit

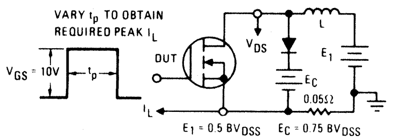


Fig. 16 — Clamped Inductive Waveforms

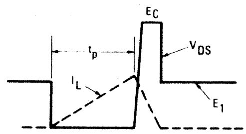


Fig. 17 — Switching Time Test Circuit

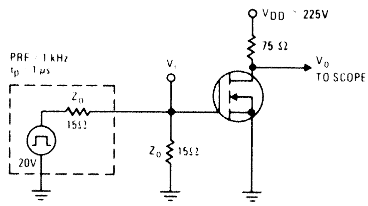
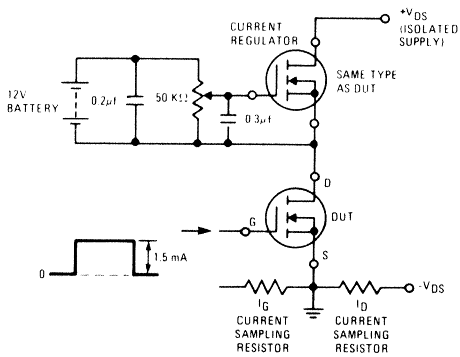


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

100 Volt, 0.3 Ohm
N-Channel

UFN120
UFN121
UFN122
UFN123

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

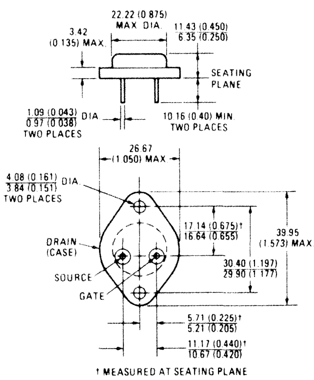
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN120	100V	0.30Ω	8.0A
UFN121	60V	0.30Ω	8.0A
UFN122	100V	0.40Ω	7.0A
UFN123	60V	0.40Ω	7.0A

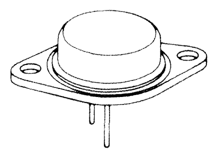
MECHANICAL SPECIFICATIONS

UFN120 UFN121 UFN122 UFN123



Dimensions in Millimeters and (Inches)

TO-3

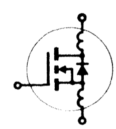


UNITRODE

ABSOLUTE MAXIMUM RATINGS

	Parameter	UFN120	UFN121	UFN122	UFN123	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_D @ T_C = 100°C	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_{DM}	Pulsed Drain Current ③	32	32	28	28	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 32	32	28	28	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	–55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

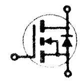
ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFN120 UFN122	100	–	–	V	V_{GS} = 0V
		UFN121 UFN123	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFN120 UFN121	8.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)\,max.}$, V_{GS} = 10V
		UFN122 UFN123	7.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFN120 UFN121	–	0.25	0.30	Ω	V_{GS} = 10V, I_D = 4.0A
		UFN122 UFN123	–	0.30	0.40	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.5	2.9	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)\,max.}$, I_D = 4.0A
C_{iss}	Input Capacitance	ALL	–	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	200	400	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	50	100	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 4.0A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	35	70	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	35	70	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	10	15	nC	V_{GS} = 10V, I_D = 10A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	6.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	4.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die. / Modified MOSFET symbol showing the internal device inductances. 
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN120 UFN121	—	—	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFN122 UFN123	—	—	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN120 UFN121	—	—	32	A	
		UFN122 UFN123	—	—	28	A	
V_{SD}	Diode Forward Voltage ②	UFN120 UFN121	—	—	2.5	V	$T_C = 25°C, I_S = 8.0A, V_{GS} = 0V$
		UFN122 UFN123	—	—	2.3	V	$T_C = 25°C, I_S = 7.0A, V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	280	—	ns	$T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	1.6	—	μC	$T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25°C$ to $150°C$. ② Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

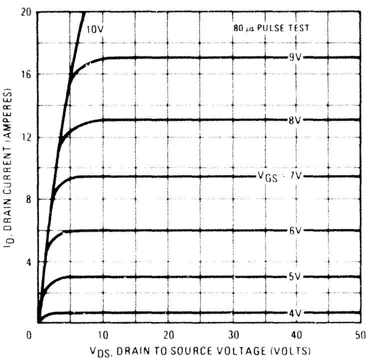


Fig. 2 — Typical Transfer Characteristics

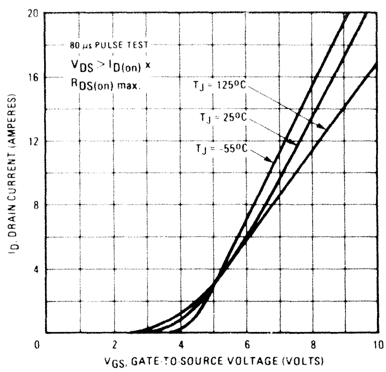


Fig. 3 — Typical Saturation Characteristics

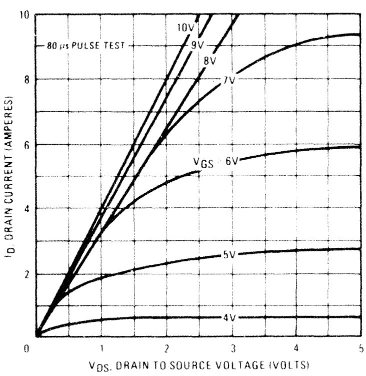


Fig. 4 — Maximum Safe Operating Area

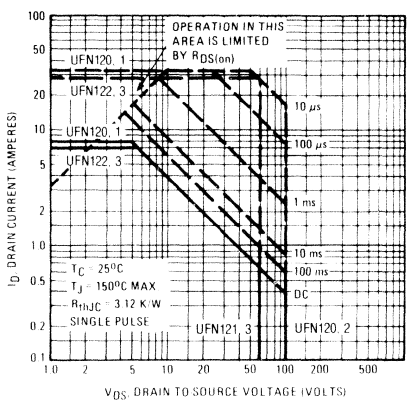


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

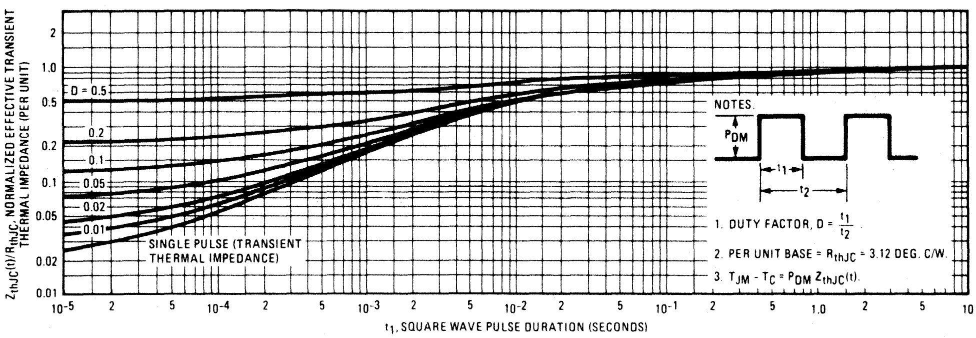


Fig. 6 — Typical Transconductance Vs. Drain Current

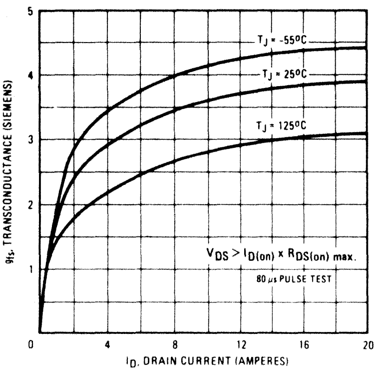


Fig. 7 — Typical Source-Drain Diode Forward Voltage

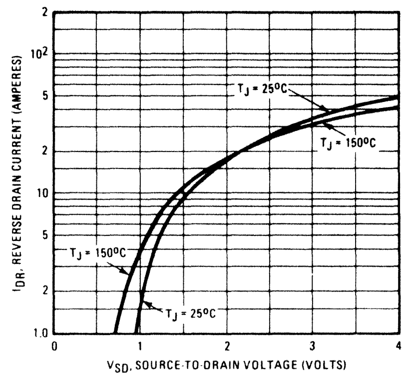


Fig. 8 — Breakdown Voltage Vs. Temperature

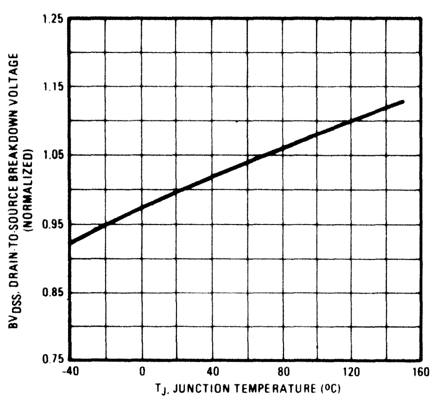


Fig. 9 — Normalized On-Resistance Vs. Temperature

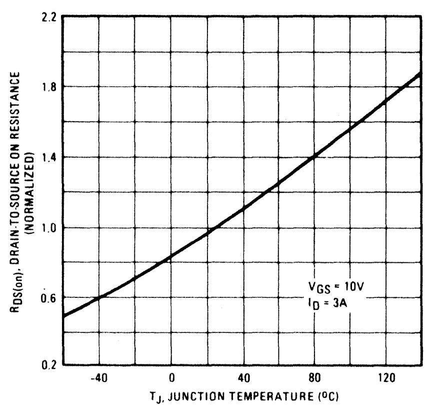


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

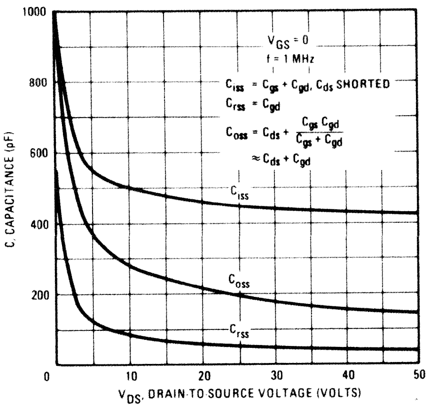


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

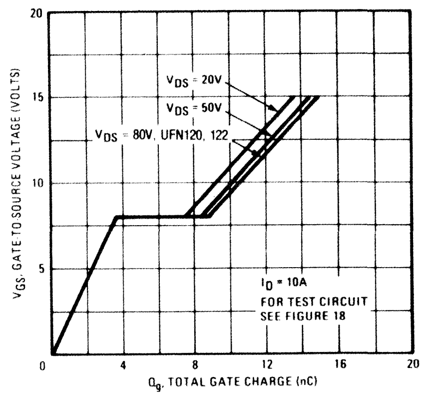


Fig. 12 — Typical On-Resistance Vs. Drain Current

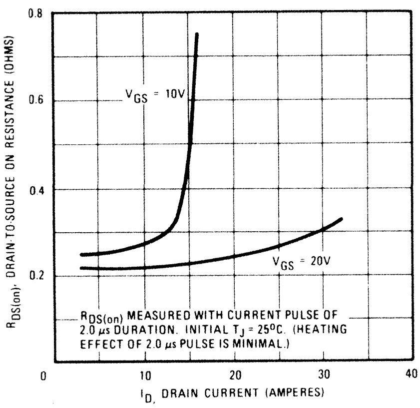


Fig. 13 — Maximum Drain Current Vs. Case Temperature

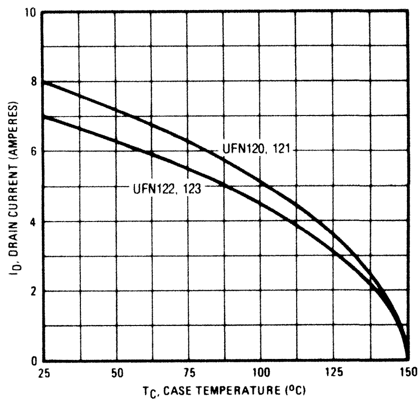


Fig. 14 — Power Vs. Temperature Derating Curve

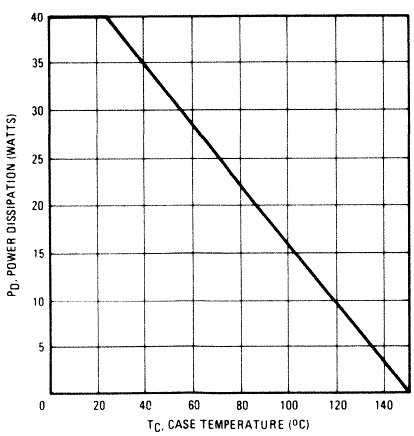


Fig. 15 — Clamped Inductive Test Circuit

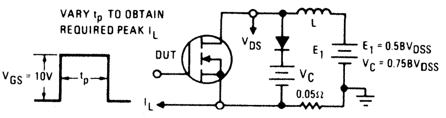


Fig. 16 — Clamped Inductive Waveforms

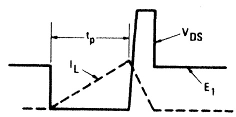


Fig. 17 — Switching Time Test Circuit

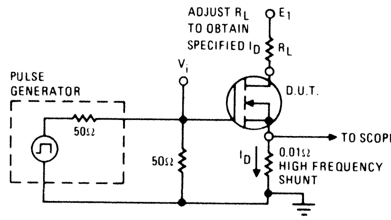
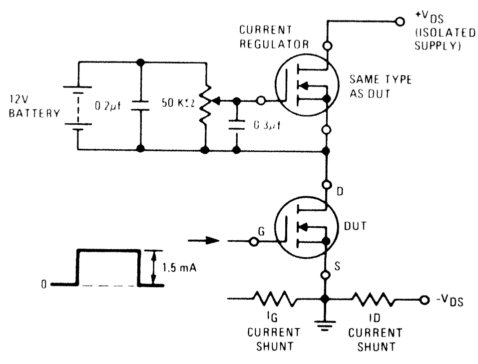


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

100 Volt, 0.18 Ohm
N-Channel

UFN130
UFN131
UFN132
UFN133

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

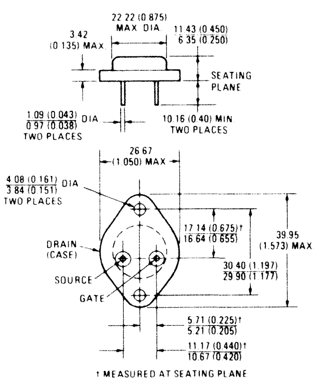
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN130	100V	0.18Ω	14A
UFN131	60V	0.18Ω	14A
UFN132	100V	0.25Ω	12A
UFN133	60V	0.25Ω	12A

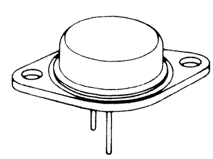
MECHANICAL SPECIFICATIONS

UFN130 UFN131 UFN132 UFN133



Dimensions in Millimeters and (Inches)

TO-3

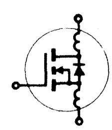


ABSOLUTE MAXIMUM RATINGS

	Parameter	UFN130	UFN131	UFN132	UFN133	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	14	14	12	12	A
I_D @ T_C = 100°C	Continuous Drain Current	9.0	9.0	8.0	8.0	A
I_{DM}	Pulsed Drain Current ③	56	56	48	48	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped (See Fig. 15 and 16) L = 100µH	56	56	48	48	A
T_J, T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

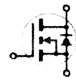
Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFN130 UFN132	100	–	–	V	V_{GS} = 0V
		UFN131 UFN133	60	–	–	V	I_D = 250µA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	µA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	µA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFN130 UFN131	14	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		UFN132 UFN133	12	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFN130 UFN131	–	0.14	0.18	Ω	V_{GS} = 10V, I_D = 8.0A
		UFN132 UFN133	–	0.20	0.25	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	5.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 8.0A
C_{iss}	Input Capacitance	ALL	–	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	300	500	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	100	150	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} ≈ 36V, I_D = 8.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	75	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	40	ns	
t_f	Fall Time	ALL	–	–	45	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	18	30	nC	V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	9.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	9.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die. / Modified MOSFET symbol showing the internal device inductances.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.



THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN130 UFN131	—	—	14	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFN132 UFN133	—	—	12	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN130 UFN131	—	—	56	A	
		UFN132 UFN133	—	—	48	A	
V_{SD}	Diode Forward Voltage ②	UFN130 UFN131	—	—	2.5	V	$T_C = 25°C, I_S = 14A, V_{GS} = 0V$
		UFN132 UFN133			2.3	V	$T_C = 25°C, I_S = 12A, V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	360	—	ns	$T_J = 150°C, I_F = 14A, dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	2.1	—	μC	$T_J = 150°C, I_F = 14A, dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25°C$ to $150°C$. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

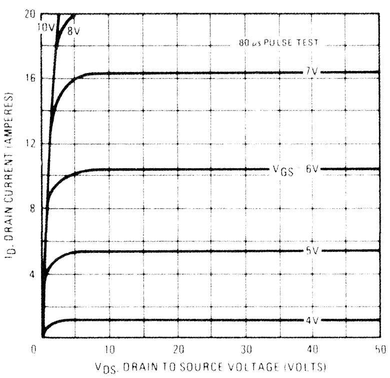


Fig. 2 — Typical Transfer Characteristics

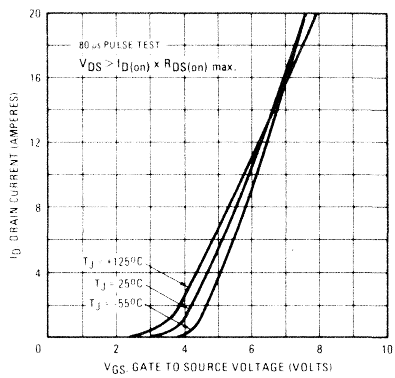


Fig. 3 — Typical Saturation Characteristics

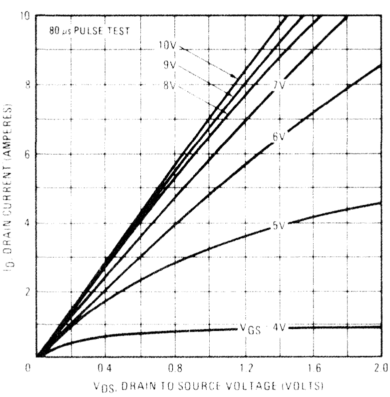


Fig. 4 — Maximum Safe Operating Area

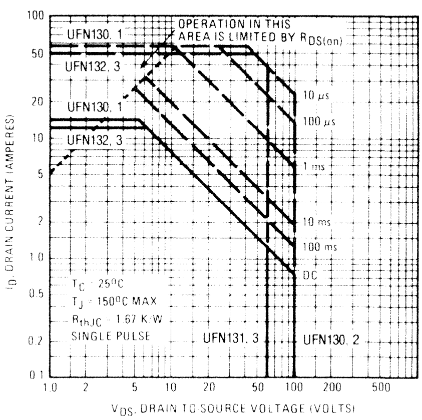


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Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

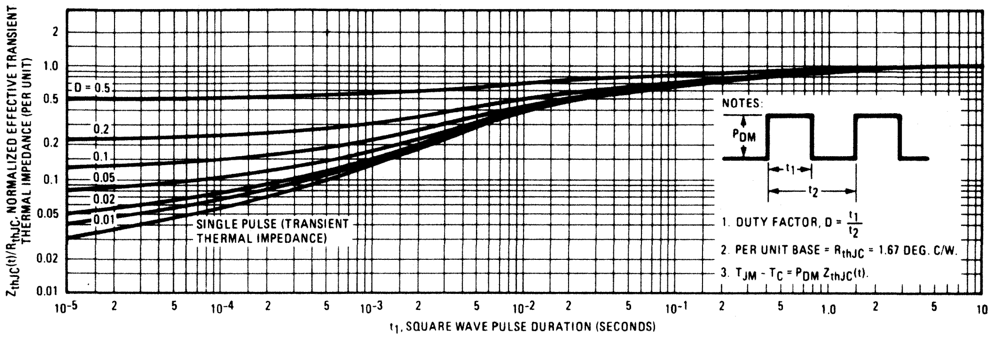


Fig. 6 — Typical Transconductance Vs. Drain Current

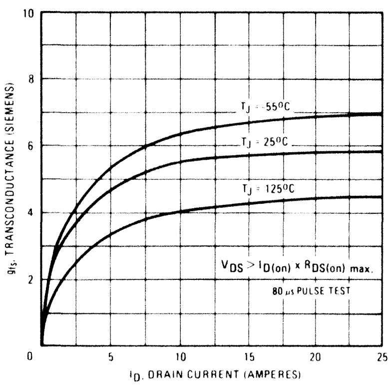


Fig. 7 — Typical Source-Drain Diode Forward Voltage

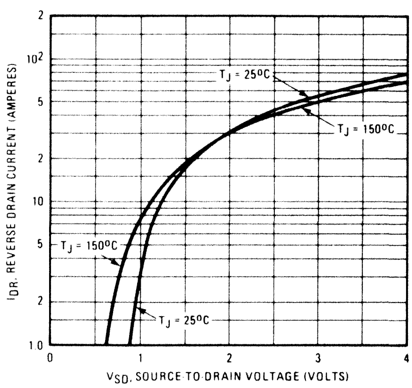


Fig. 8 — Breakdown Voltage Vs. Temperature

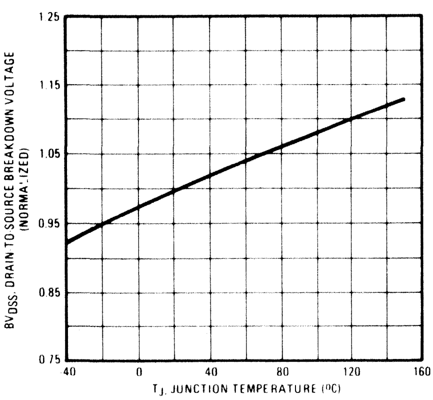


Fig. 9 — Normalized On-Resistance Vs. Temperature

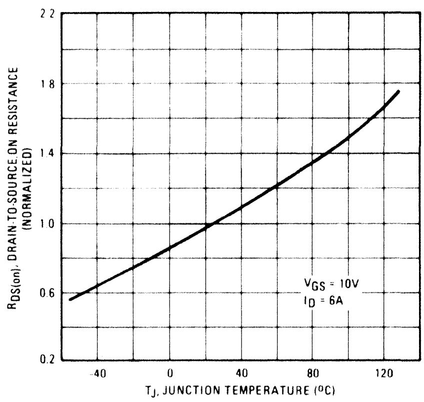


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

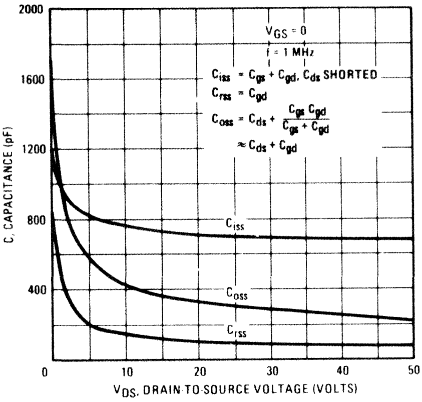


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

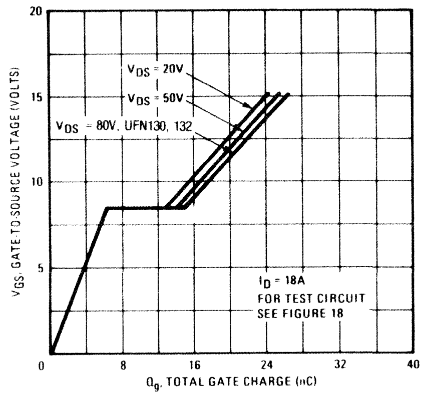


Fig. 12 — Typical On-Resistance Vs. Drain Current

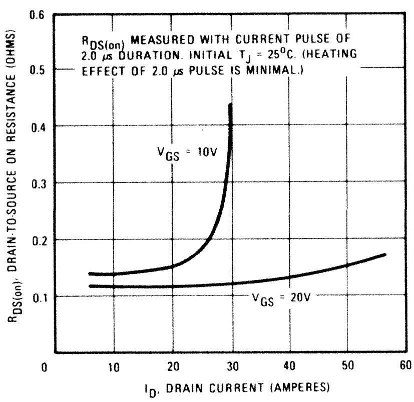


Fig. 13 — Maximum Drain Current Vs. Case Temperature

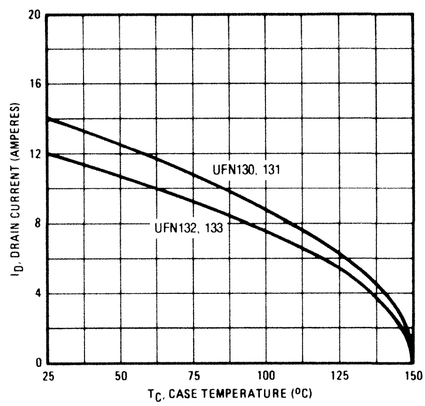


Fig. 14 — Power Vs. Temperature Derating Curve

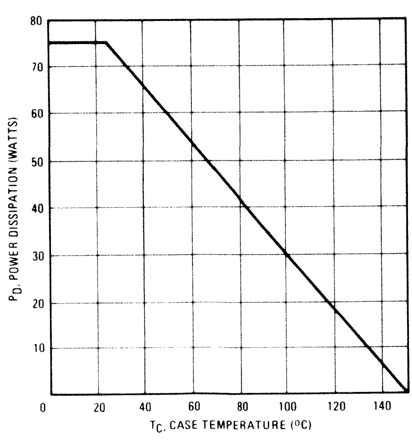


Fig. 15 — Clamped Inductive Test Circuit

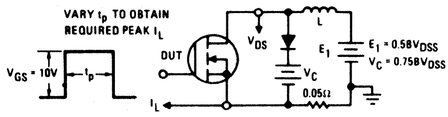


Fig. 16 — Clamped Inductive Waveforms

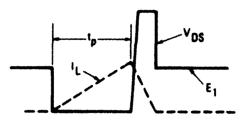


Fig. 17 — Switching Time Test Circuit

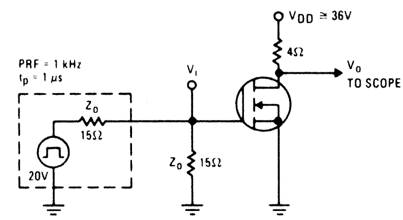
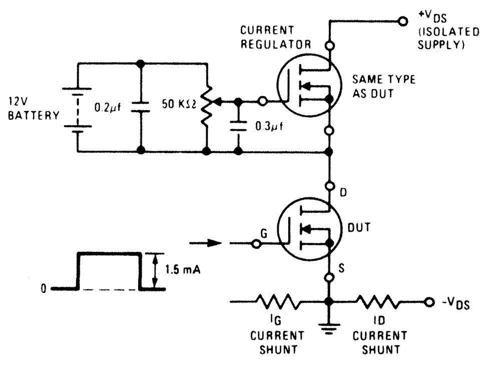


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

100 Volt, 0.085 Ohm
N-Channel

UFN140
UFN141
UFN142
UFN143

FEATURES
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION
The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

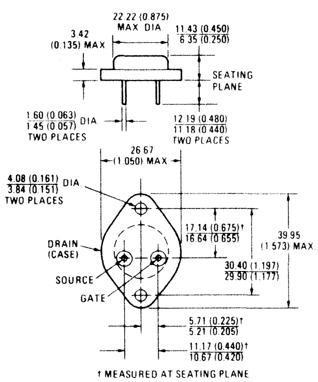
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN140	100V	0.085Ω	27A
UFN141	60V	0.085Ω	27A
UFN142	100V	0.11Ω	24A
UFN143	60V	0.11Ω	24A

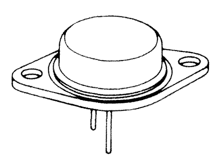
MECHANICAL SPECIFICATIONS

UFN140 UFN141 UFN142 UFN143



Dimensions in Millimeters and (Inches)

TO-3 (Modified)



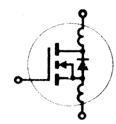
UNITRODE

ABSOLUTE MAXIMUM RATINGS

Parameter		UFN140	UFN141	UFN142	UFN143	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	27	27	24	24	A
I_D @ T_C = 100°C	Continuous Drain Current	17	17	15	15	A
I_{DM}	Pulsed Drain Current ③	108	108	96	96	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped (See Fig. 15 and 16) L = 100μH	108	108	96	96	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

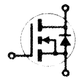
Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFN140 UFN142	100	—	—	V	V_{GS} = 0V
		UFN141 UFN143	60	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFN140 UFN141	27	—	—	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		UFN142 UFN143	24	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFN140 UFN141	—	0.07	0.085	Ω	V_{GS} = 10V, I_D = 15A
		UFN142 UFN143	—	0.09	0.11	Ω	
g_{fs}	Forward Transconductance ②	ALL	6.0	10	—	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 15A
C_{iss}	Input Capacitance	ALL	—	1275	1600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	550	800	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	160	300	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	16	30	ns	V_{DD} = 30V, I_D = 15A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	27	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	38	80	ns	
t_f	Fall Time	ALL	—	14	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	38	60	nC	V_{GS} = 10V, I_D = 34A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	17	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	21	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die. / Modified MOSFET symbol showing the internal device inductances.
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.



THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	—	—	1.0	K/W	
R_{thCS}	Case-to-Sink	ALL	—	0.1	—	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN140 UFN141	—	—	27	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFN142 UFN143	—	—	24	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN140 UFN141	—	—	108	A	
		UFN142 UFN143	—	—	96	A	
V_{SD}	Diode Forward Voltage ②	UFN140 UFN141	—	—	2.5	V	$T_C = 25°C, I_S = 27A, V_{GS} = 0V$
		UFN142 UFN143	—	—	2.3	V	$T_C = 25°C, I_S = 24A, V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	500	—	ns	$T_J = 150°C, I_F = 27A, dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	2.9	—	μC	$T_J = 150°C, I_F = 27A, dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25°C$ to $150°C$. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

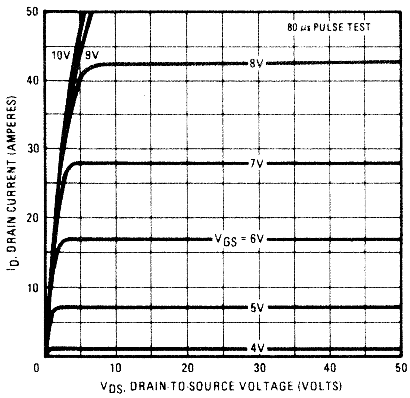


Fig. 2 — Typical Transfer Characteristics

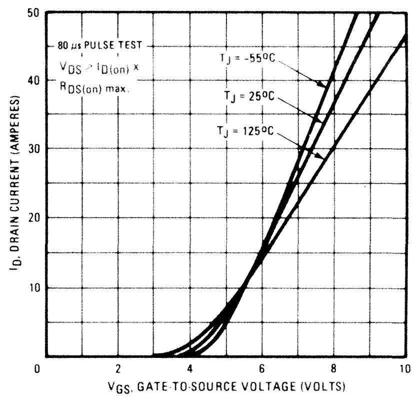


Fig. 3 — Typical Saturation Characteristics

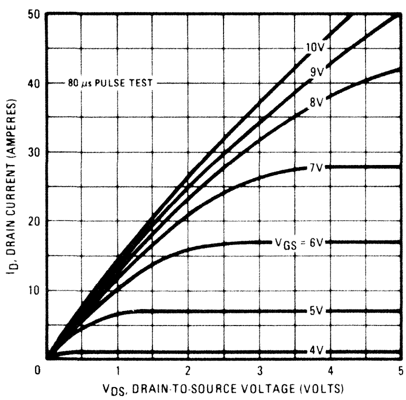


Fig. 4 — Maximum Safe Operating Area

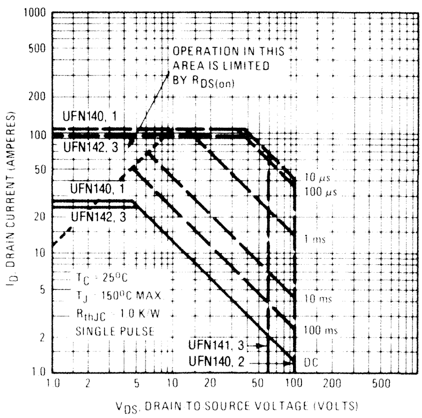


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

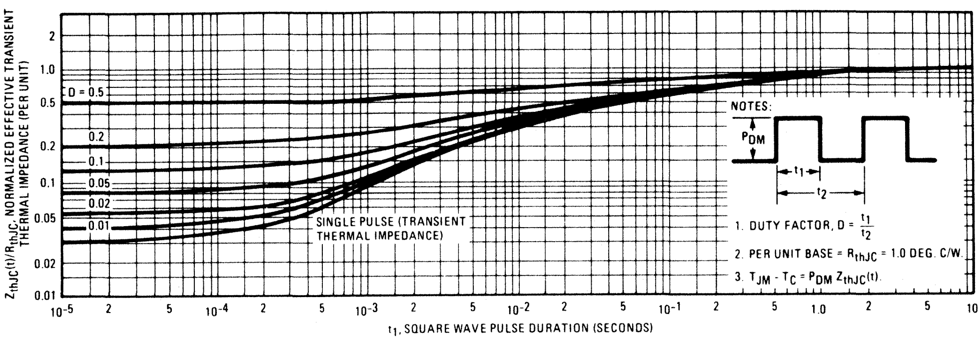


Fig. 6 — Typical Transconductance Vs. Drain Current

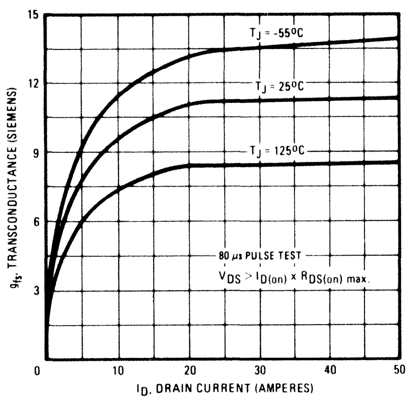


Fig. 7 — Typical Source-Drain Diode Forward Voltage

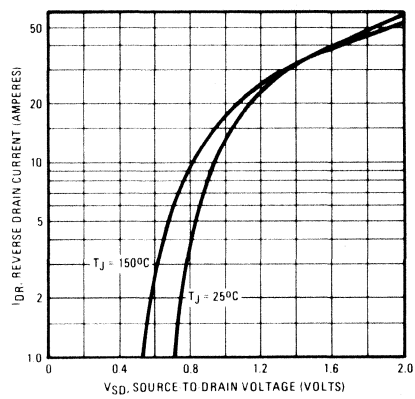


Fig. 8 — Breakdown Voltage Vs. Temperature

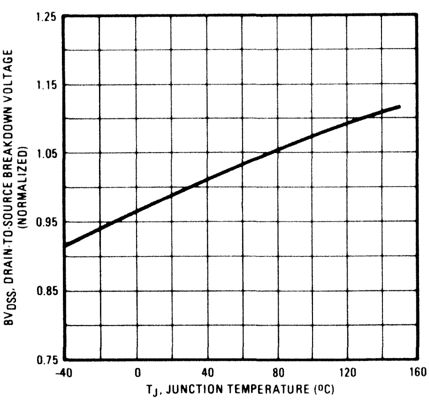


Fig. 9 — Normalized On-Resistance Vs. Temperature

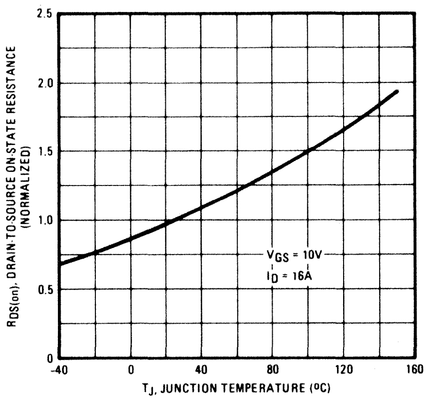


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

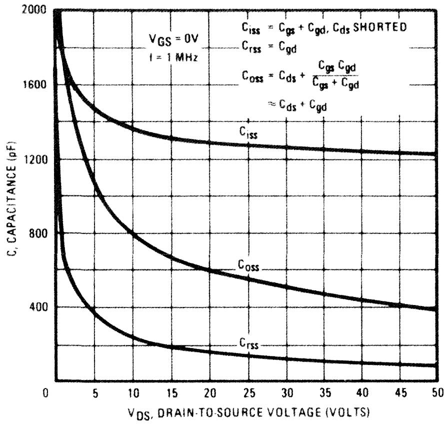


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

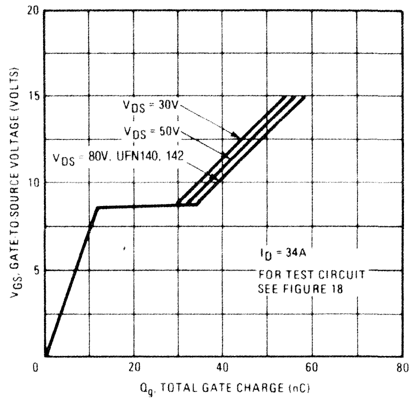


Fig. 12 — Typical On-Resistance Vs. Drain Current

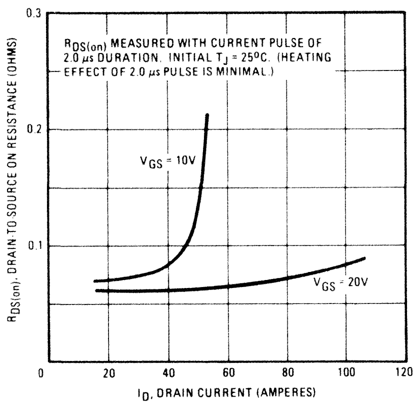


Fig. 13 — Maximum Drain Current Vs. Case Temperature

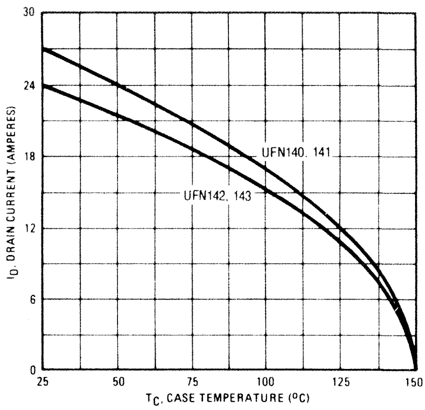


Fig. 14 — Power Vs. Temperature Derating Curve

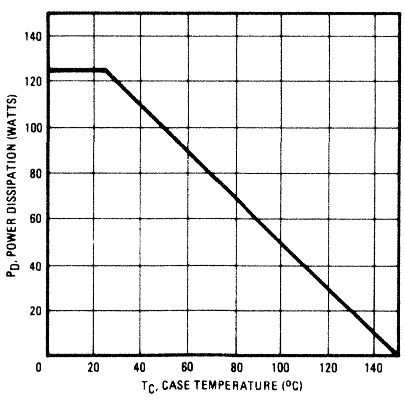


Fig. 15 — Clamped Inductive Test Circuit

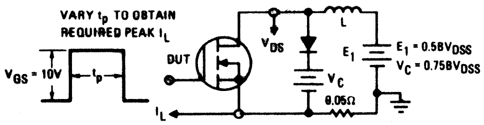


Fig. 16 — Clamped Inductive Waveforms

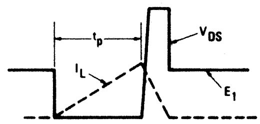


Fig. 17 — Switching Time Test Circuit

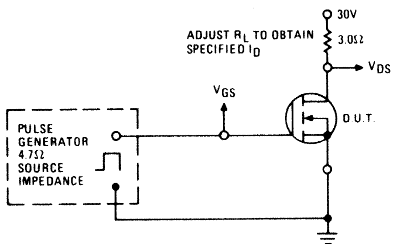
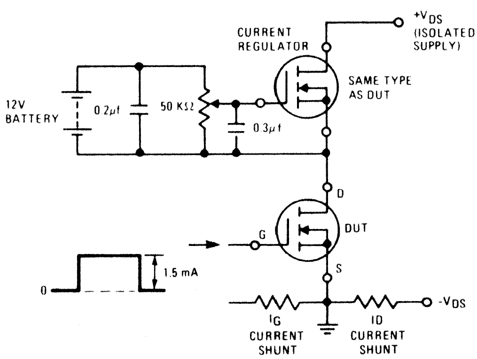


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

100 Volt, 0.055 Ohm
N-Channel

UFN150
UFN151
UFN152
UFN153

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

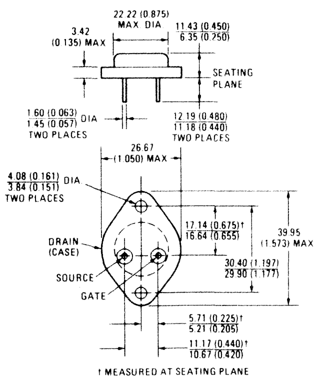
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN150	100V	0.055Ω	40A
UFN151	60V	0.055Ω	40A
UFN152	100V	0.08Ω	33A
UFN153	60V	0.08Ω	33A

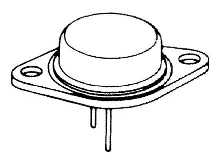
MECHANICAL SPECIFICATIONS

UFN150 UFN151 UFN152 UFN153



Dimensions in Millimeters and (Inches)

TO-3 (Modified)

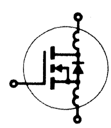


UNITRODE

ABSOLUTE MAXIMUM RATINGS

Parameter		UFN150	UFN151	UFN152	UFN153	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	40	40	33	33	A
I_D @ T_C = 100°C	Continuous Drain Current	25	25	20	20	A
I_{DM}	Pulsed Drain Current ③	160	160	132	132	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	150 (See Fig. 14)				W
	Linear Derating Factor	1.2 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 160	160	132	132	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

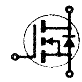
ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFN150 UFN152	100	–	–	V	V_{GS} = 0V
		UFN151 UFN153	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFN150 UFN151	40	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\,max.}$, V_{GS} = 10V
		UFN152 UFN153	33	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFN150 UFN151	–	0.045	0.055	Ω	V_{GS} = 10V, I_D = 20A
		UFN152 UFN153	–	0.06	0.08	Ω	
g_{fs}	Forward Transconductance ②	ALL	9.0	11	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)\,max.}$, I_D = 20A
C_{iss}	Input Capacitance	ALL	–	2000	3000	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	1000	1500	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	350	500	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	35	ns	V_{DD} = 24V, I_D = 20A, Z_o = 4.7Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	100	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	125	ns	
t_f	Fall Time	ALL	–	–	100	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	63	120	nC	V_{GS} = 10V, I_D = 50A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	27	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	36	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die. — Modified MOSFET symbol showing the internal device inductances. 
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	0.83	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN150 UFN151	—	—	40	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFN152 UFN153	—	—	33	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN150 UFN151	—	—	160	A	
		UFN152 UFN153	—	—	132	A	
V_{SD}	Diode Forward Voltage ②	UFN150 UFN151	—	—	2.5	V	T_C = 25°C, I_S = 40A, V_{GS} = 0V
		UFN152 UFN153	—	—	2.3	V	T_C = 25°C, I_S = 33A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	600	—	ns	T_J = 150°C, I_F = 40A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	3.3	—	μC	T_J = 150°C, I_F = 40A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

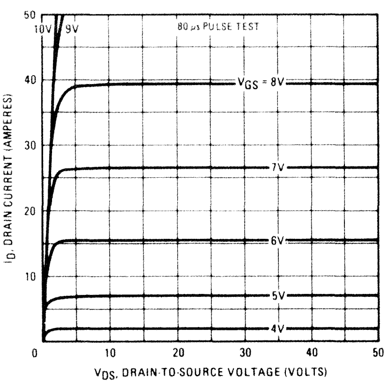


Fig. 2 — Typical Transfer Characteristics

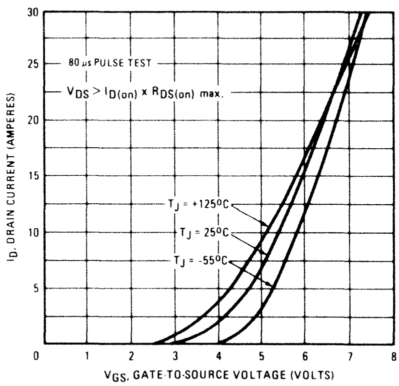


Fig. 3 — Typical Saturation Characteristics

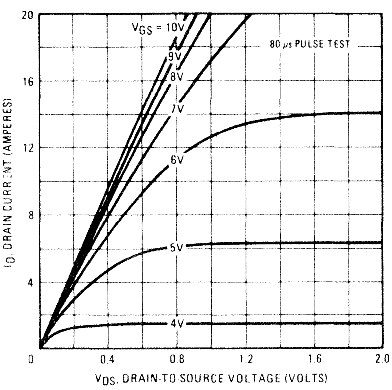


Fig. 4 — Maximum Safe Operating Area

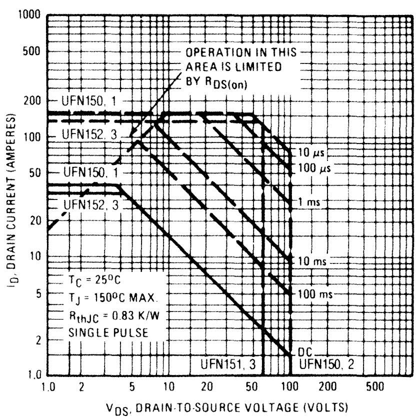


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

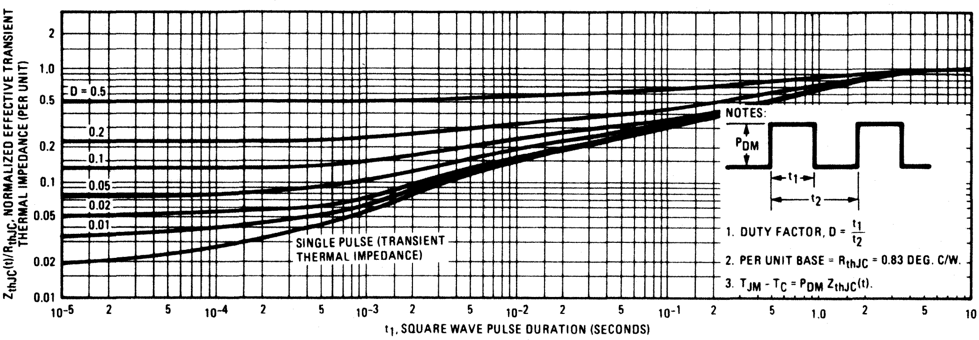


Fig. 6 — Typical Transconductance Vs. Drain Current

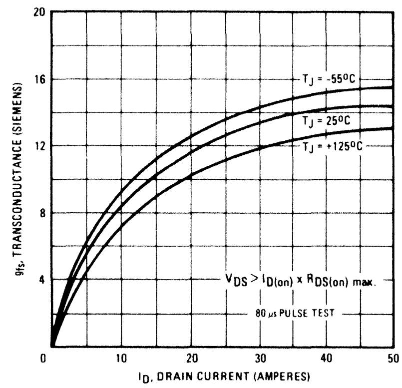


Fig. 7 — Typical Source-Drain Diode Forward Voltage

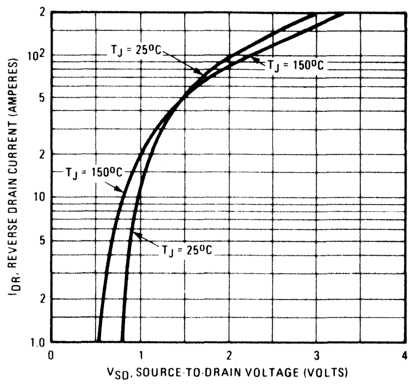


Fig. 8 — Breakdown Voltage Vs. Temperature

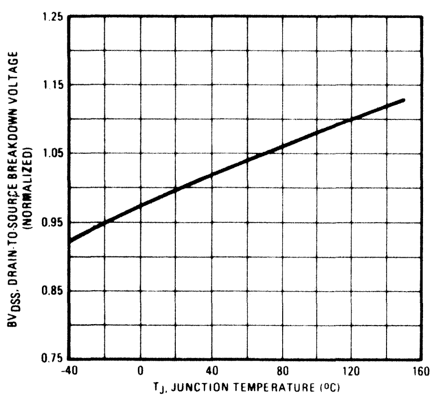


Fig. 9 — Normalized On-Resistance Vs. Temperature

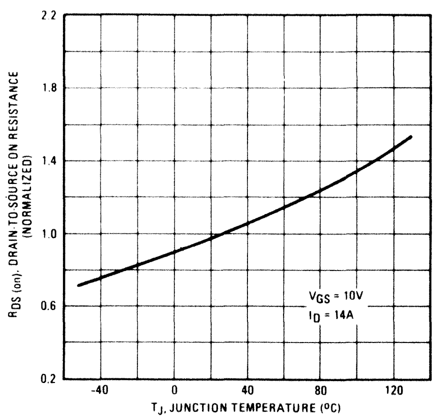


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

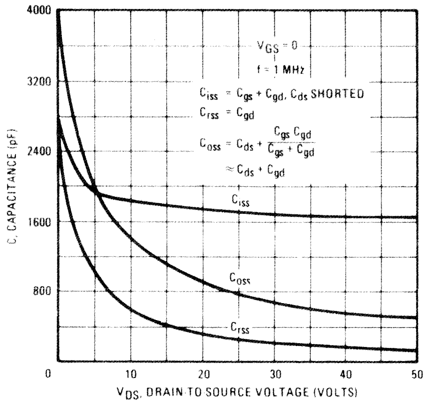


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

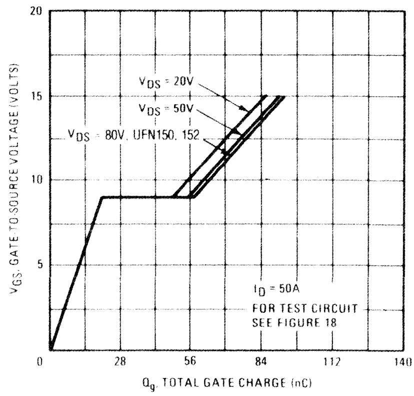


Fig. 12 – Typical On-Resistance Vs. Drain Current

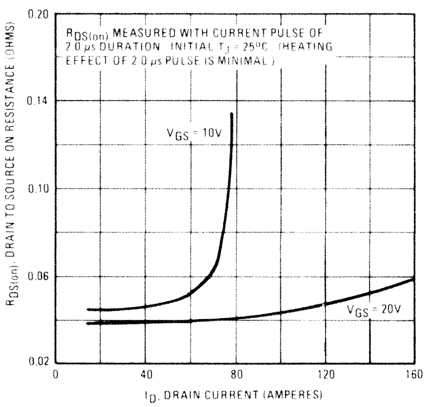


Fig. 13 – Maximum Drain Current Vs. Case Temperature

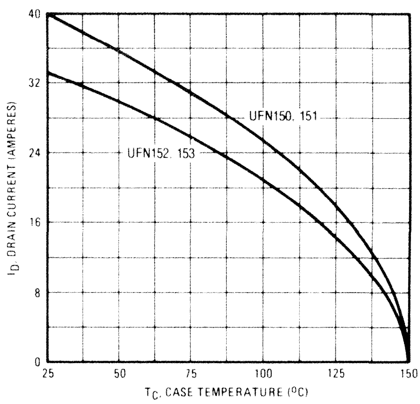


Fig. 14 – Power Vs. Temperature Derating Curve

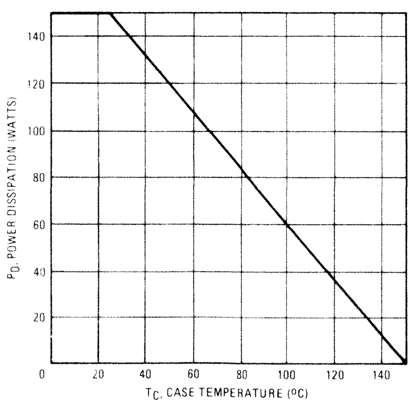


Fig. 15 — Clamped Inductive Test Circuit

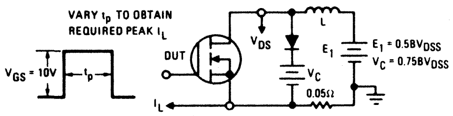


Fig. 16 — Clamped Inductive Waveforms

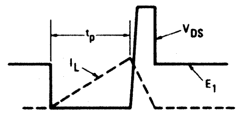


Fig. 17 — Switching Time Test Circuit

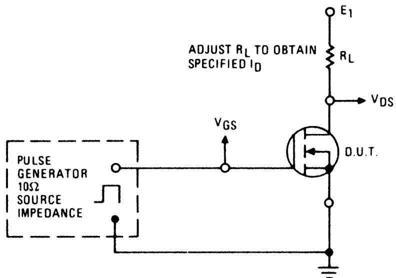
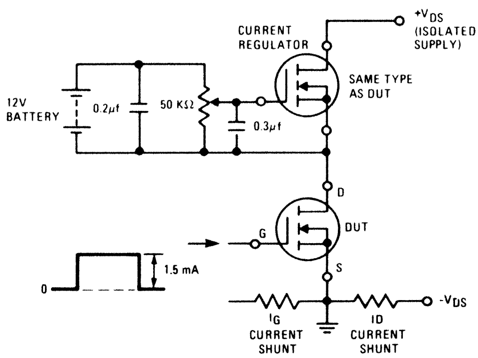


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

200 Volt, 0.8 Ohm
N-Channel

UFN220
UFN221
UFN222
UFN223

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

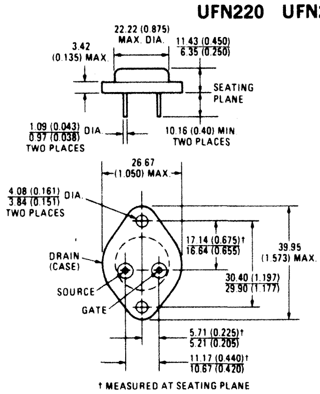
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN220	200V	0.8Ω	5.0A
UFN221	150V	0.8Ω	5.0A
UFN222	200V	1.2Ω	4.0A
UFN223	150V	1.2Ω	4.0A

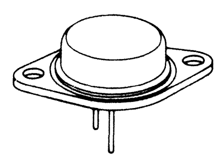
MECHANICAL SPECIFICATIONS

UFN220 UFN221 UFN222 UFN223



Dimensions in Millimeters and (Inches)

TO-3

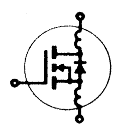


UNITRODE

ABSOLUTE MAXIMUM RATINGS

	Parameter	UFN220	UFN221	UFN222	UFN223	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_D @ T_C = 100°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_{DM}	Pulsed Drain Current ③	20	20	16	16	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 20	20	16	16	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-50 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

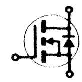
ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFN220 UFN222	200	–	–	V	V_{GS} = 0V
		UFN221 UFN223	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFN220 UFN221	5.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)\,max.}$, V_{GS} = 10V
		UFN222 UFN223	4.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFN220 UFN221	–	0.5	0.8	Ω	V_{GS} = 10V, I_D = 2.5A
		UFN222 UFN223	–	0.8	1.2	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.3	2.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)\,max.}$, I_D = 2.5A
C_{iss}	Input Capacitance	ALL	–	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	150	300	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	40	80	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 2.5A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	30	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	30	60	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	11	15	nC	V_{GS} = 10V, I_D = 6.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	5.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	6.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die. / Modified MOSFET symbol showing the internal device inductances.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad. 

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN220 UFN221	—	—	5.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFN222 UFN223	—	—	4.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN220 UFN221	—	—	20	A	
		UFN222 UFN223	—	—	16	A	
V_{SD}	Diode Forward Voltage ②	UFN220 UFN221	—	—	2.0	V	$T_C = 25°C, I_S = 5.0A, V_{GS} = 0V$
		UFN222 UFN223	—	—	1.8	V	$T_C = 25°C, I_S = 4.0A, V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	350	—	ns	$T_J = 150°C, I_F = 5.0A, dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	2.3	—	μC	$T_J = 150°C, I_F = 5.0A, dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25°C$ to $150°C$. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

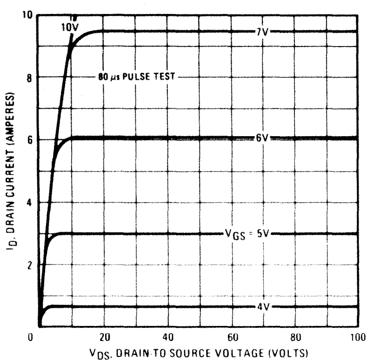


Fig. 2 — Typical Transfer Characteristics

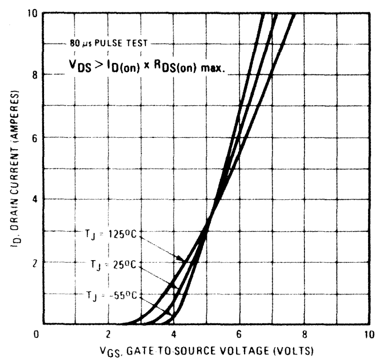


Fig. 3 — Typical Saturation Characteristics

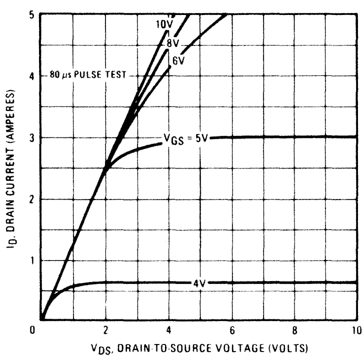


Fig. 4 — Maximum Safe Operating Area

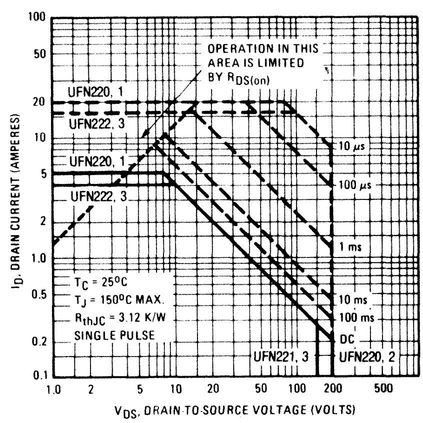


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Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

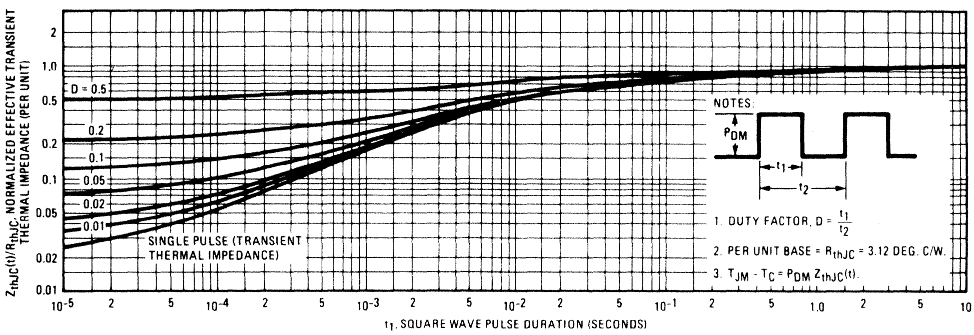


Fig. 6 — Typical Transconductance Vs. Drain Current

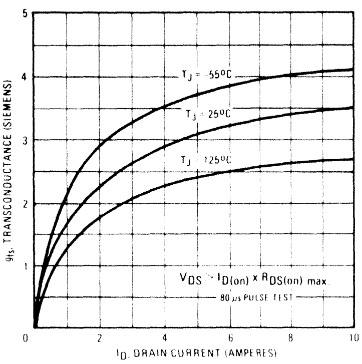


Fig. 7 — Typical Source-Drain Diode Forward Voltage

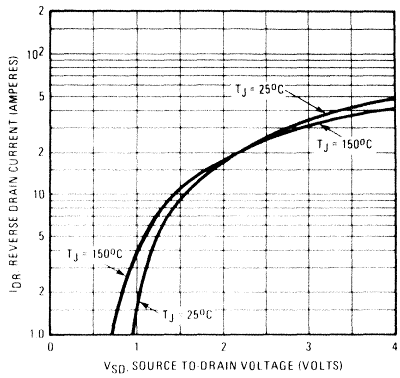


Fig. 8 — Breakdown Voltage Vs. Temperature

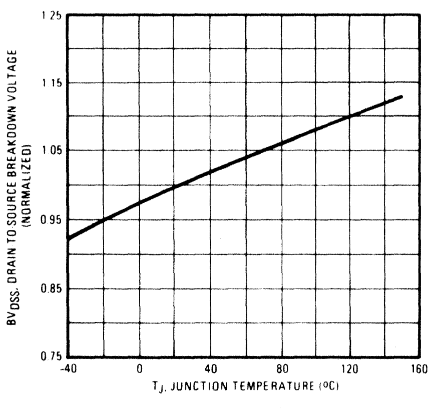


Fig. 9 — Normalized On-Resistance Vs. Temperature

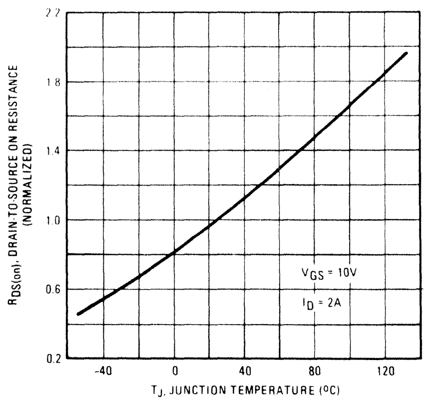


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

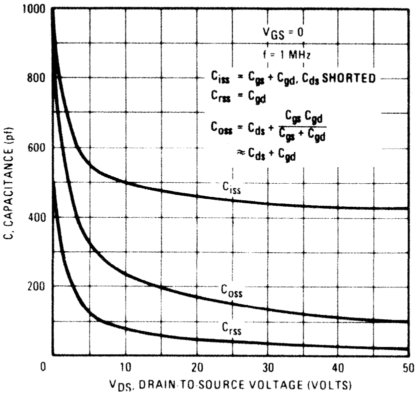


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

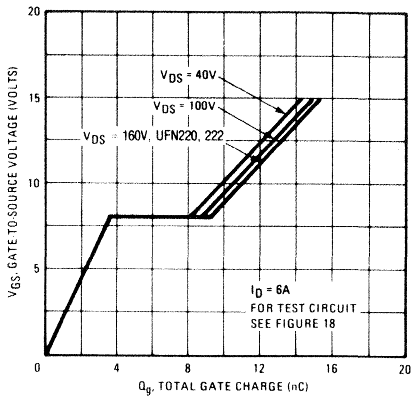


Fig. 12 — Typical On-Resistance Vs. Drain Current

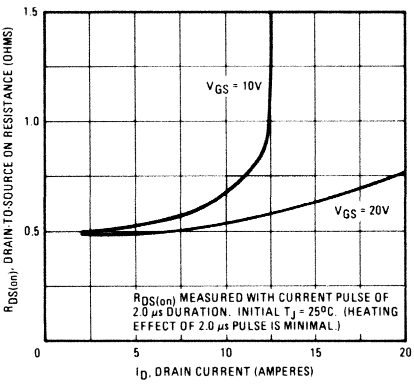


Fig. 13 — Maximum Drain Current Vs. Case Temperature

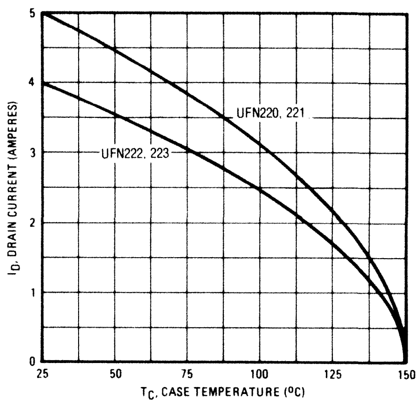


Fig. 14 — Power Vs. Temperature Derating Curve

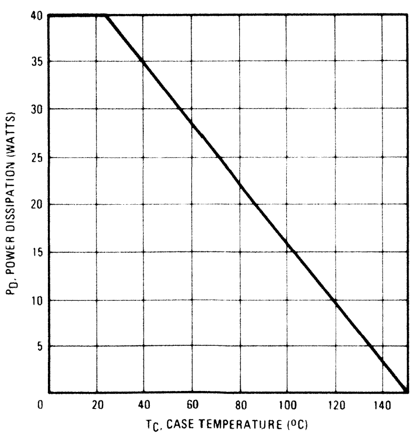


Fig. 15 — Clamped Inductive Test Circuit

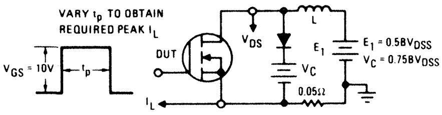


Fig. 16 — Clamped Inductive Waveforms

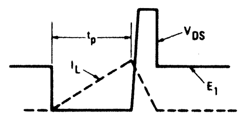


Fig. 17 — Switching Time Test Circuit

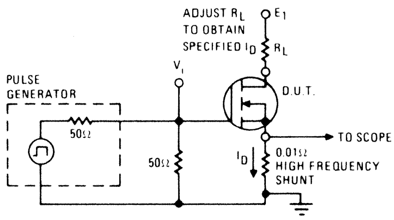
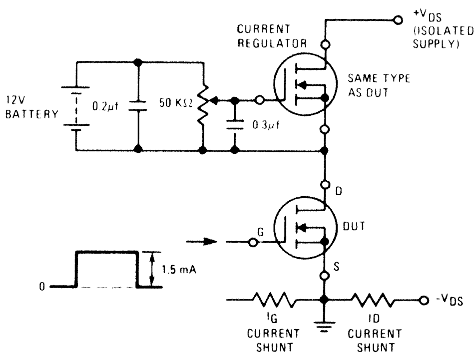


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

200 Volt, 0.4 Ohm
N-Channel

UFN230
UFN231
UFN232
UFN233

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

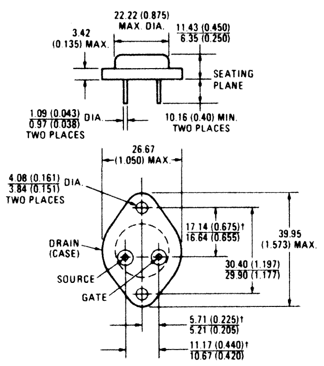
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN230	200V	0.4Ω	9.0A
UFN231	150V	0.4Ω	9.0A
UFN232	200V	0.6Ω	8.0A
UFN233	150V	0.6Ω	8.0A

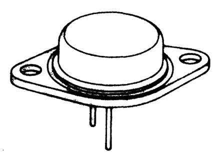
MECHANICAL SPECIFICATIONS

UFN230 UFN231 UFN232 UFN233



Dimensions in Millimeters and (Inches)

TO-3

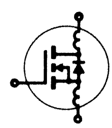


UNITRODE

ABSOLUTE MAXIMUM RATINGS

	Parameter	UFN230	UFN231	UFN232	UFN233	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	9.0	9.0	8.0	8.0	A
I_D @ T_C = 100°C	Continuous Drain Current	6.0	6.0	5.0	5.0	A
I_{DM}	Pulsed Drain Current ③	36	36	32	32	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 36	36	32	32	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

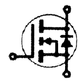
ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFN230 UFN232	200	–	–	V	V_{GS} = 0V
		UFN231 UFN233	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFN230 UFN231	9.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		UFN232 UFN233	8.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFN230 UFN231	–	0.25	0.4	Ω	V_{GS} = 10V, I_D = 5.0A
		UFN232 UFN233	–	0.4	0.6	Ω	
g_{fs}	Forward Transconductance ②	ALL	3.0	4.8	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 5.0A
C_{iss}	Input Capacitance	ALL	–	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	250	450	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	80	150	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} ≈ 90V, I_D = 5.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	50	ns	
t_f	Fall Time	ALL	–	–	40	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	19	30	nC	V_{GS} = 10V, I_D = 12A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	10	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	9.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die. — Modified MOSFET symbol showing the internal device inductances.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad. 

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN230 UFN231	–	–	9.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFN232 UFN233	–	–	8.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN230 UFN231	–	–	36	A	
		UFN232 UFN233	–	–	32	A	
V_{SD}	Diode Forward Voltage ②	UFN230 UFN231	–	–	2.0	V	$T_C = 25°C, I_S = 9.0A, V_{GS} = 0V$
		UFN232 UFN233	–	–	1.8	V	$T_C = 25°C, I_S = 8.0A, V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	–	450	–	ns	$T_J = 150°C, I_F = 9.0A, dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	–	3.0	–	μC	$T_J = 150°C, I_F = 9.0A, dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

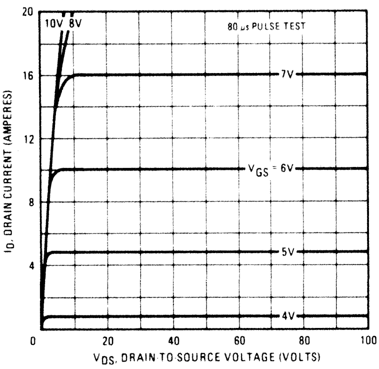


Fig. 2 — Typical Transfer Characteristics

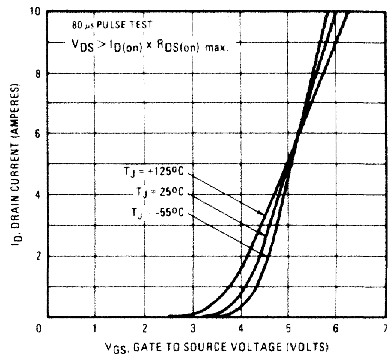


Fig. 3 — Typical Saturation Characteristics

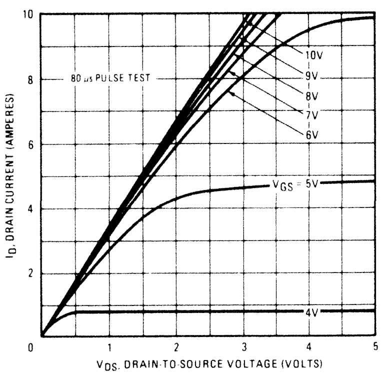
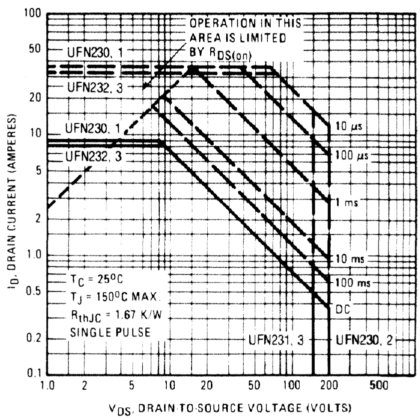


Fig. 4 — Maximum Safe Operating Area



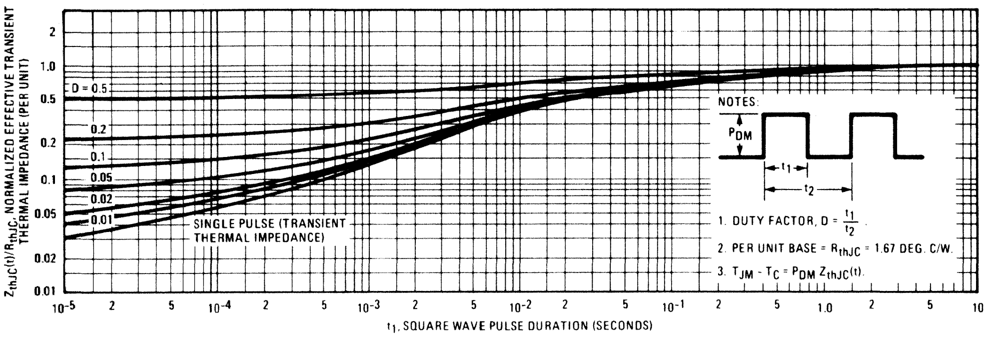


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

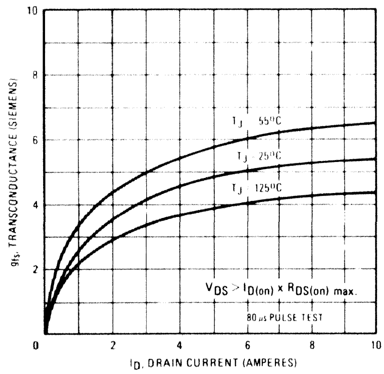


Fig. 6 — Typical Transconductance Vs. Drain Current

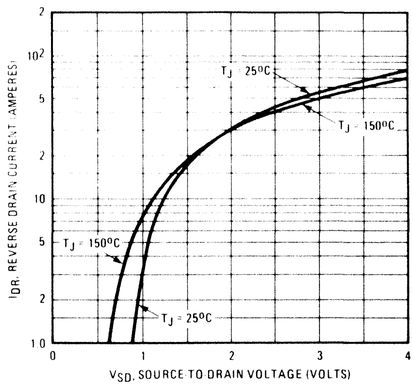


Fig. 7 — Typical Source-Drain Diode Forward Voltage

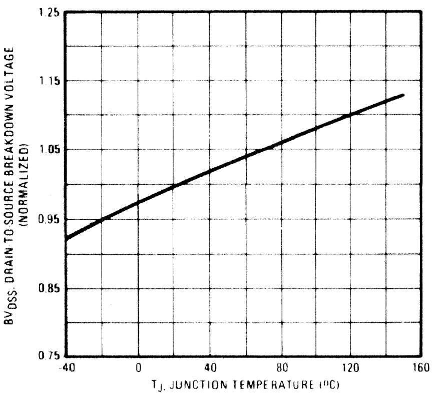


Fig. 8 — Breakdown Voltage Vs. Temperature

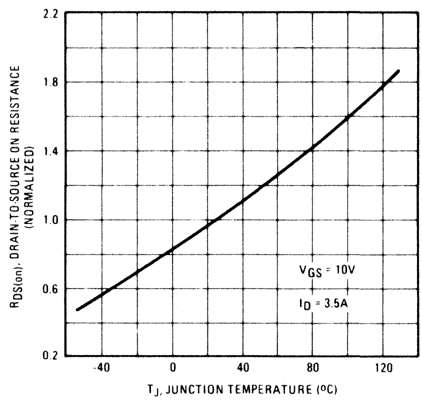


Fig. 9 — Normalized On-Resistance Vs. Temperature

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Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

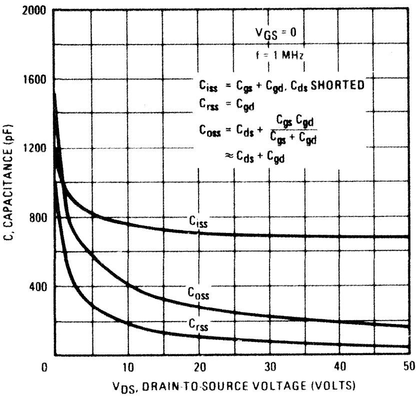


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

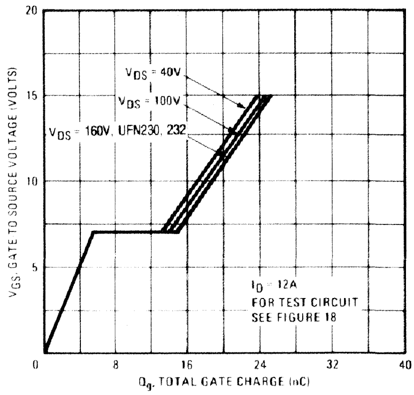


Fig. 12 – Typical On-Resistance Vs. Drain Current

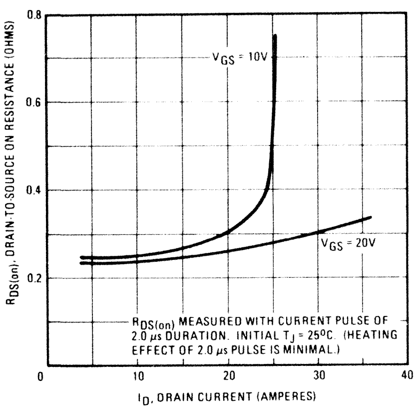


Fig. 13 – Maximum Drain Current Vs. Case Temperature

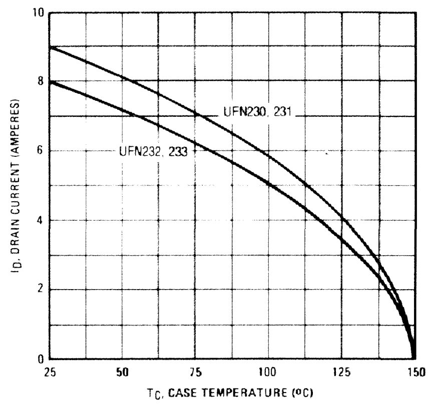


Fig. 14 – Power Vs. Temperature Derating Curve

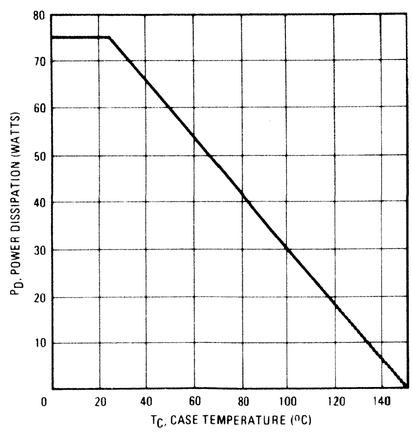


Fig. 15 – Clamped Inductive Test Circuit

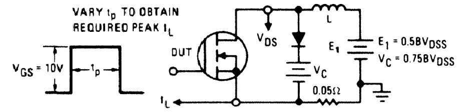


Fig. 16 – Clamped Inductive Waveforms

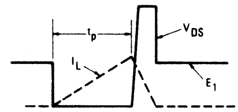


Fig. 17 – Switching Time Test Circuit

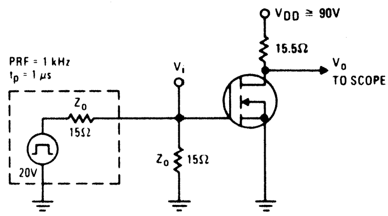
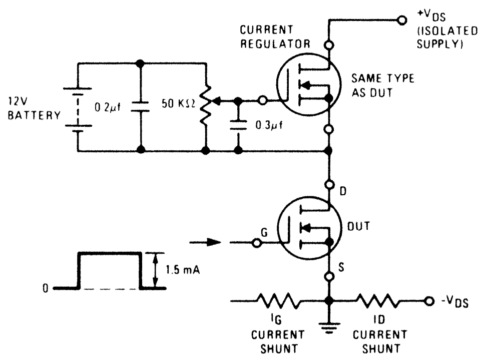


Fig. 18 – Gate Charge Test Circuit



POWER MOSFET TRANSISTORS
200 Volt, 0.2 Ohm
N-Channel

UFN240
UFN241
UFN242
UFN243

FEATURES
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

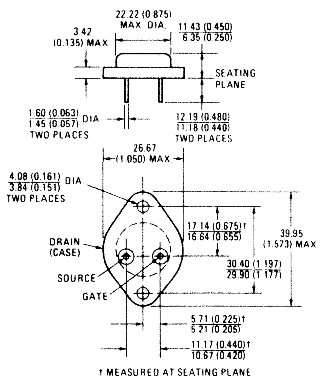
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN240	200V	0.18Ω	18A
UFN241	150V	0.18Ω	18A
UFN242	200V	0.22Ω	16A
UFN243	150V	0.22Ω	16A

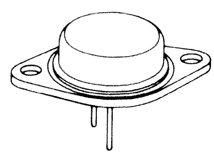
MECHANICAL SPECIFICATIONS

UFN240 UFN241 UFN242 UFN243



Dimensions in Millimeters and (Inches)

TO-3 (Modified)

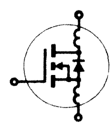


UNITRODE

ABSOLUTE MAXIMUM RATINGS

Parameter		UFN240	UFN241	UFN242	UFN243	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	18	18	16	16	A
I_D @ T_C = 100°C	Continuous Drain Current	11	11	10	10	A
I_{DM}	Pulsed Drain Current ③	72	72	64	64	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 72	72	64	64	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFN240 UFN242	200	–	–	V	V_{GS} = 0V
		UFN241 UFN243	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFN240 UFN241	18	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		UFN242 UFN243	16	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFN240 UFN241	–	0.14	0.18	Ω	V_{GS} = 10V, I_D = 10A
		UFN242 UFN243	–	0.20	0.22	Ω	
g_{fs}	Forward Transconductance ②	ALL	6.0	9.0	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 10A
C_{iss}	Input Capacitance	ALL	–	1275	1600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	500	750	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	160	300	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	16	30	ns	V_{DD} = 75V, I_D = 10A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	27	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	40	80	ns	
t_f	Fall Time	ALL	–	31	60	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	43	60	nC	V_{GS} = 10V, I_D = 22A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	16	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	27	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die. / Modified MOSFET symbol showing the internal device inductances.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad. 

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	1.0	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

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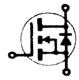
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN240 UFN241	–	–	18	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFN242 UFN243	–	–	16	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN240 UFN241	–	–	72	A	
		UFN242 UFN243	–	–	64	A	
V_{SD}	Diode Forward Voltage ②	UFN240 UFN241	–	–	2.0	V	$T_C = 25°C$, $I_S = 18A$, $V_{GS} = 0V$
		UFN242 UFN243	–	–	1.9	V	$T_C = 25°C$, $I_S = 16A$, $V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	–	650	–	ns	$T_J = 150°C$, $I_F = 18A$, $dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	–	4.1	–	μC	$T_J = 150°C$, $I_F = 18A$, $dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$				

① $T_J = 25°C$ to $150°C$. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

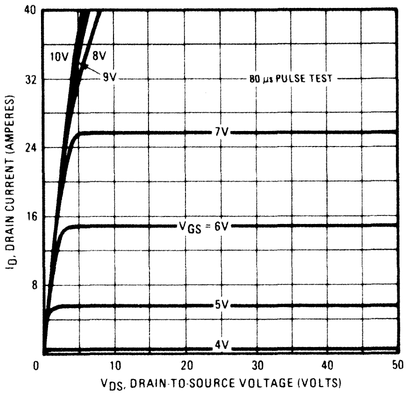


Fig. 2 – Typical Transfer Characteristics

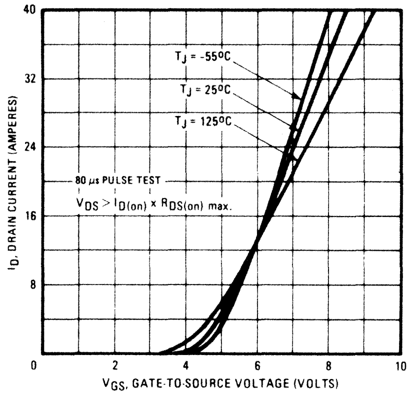


Fig. 3 – Typical Saturation Characteristics

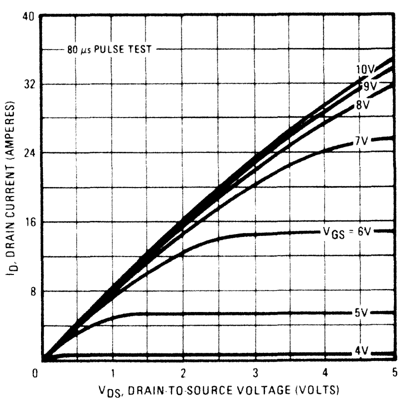


Fig. 4 – Maximum Safe Operating Area

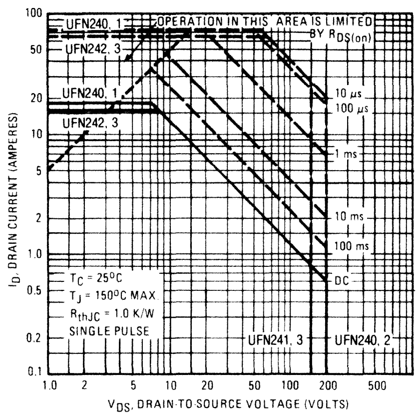


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

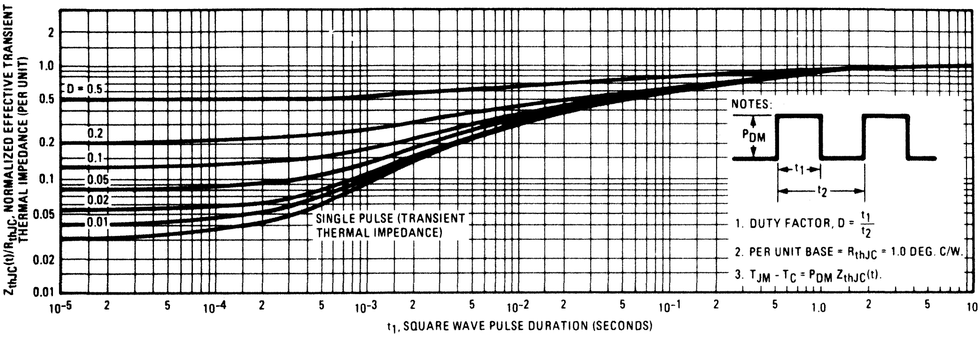


Fig. 6 — Typical Transconductance Vs. Drain Current

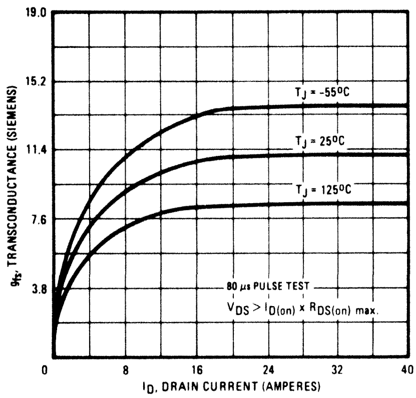


Fig. 7 — Typical Source-Drain Diode Forward Voltage

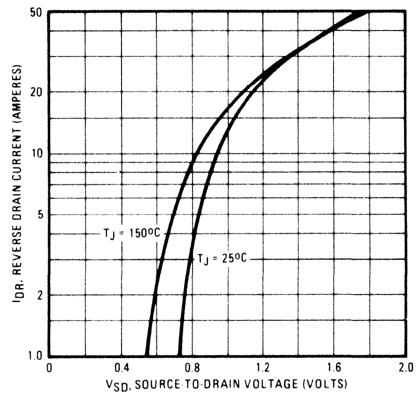


Fig. 8 — Breakdown Voltage Vs. Temperature

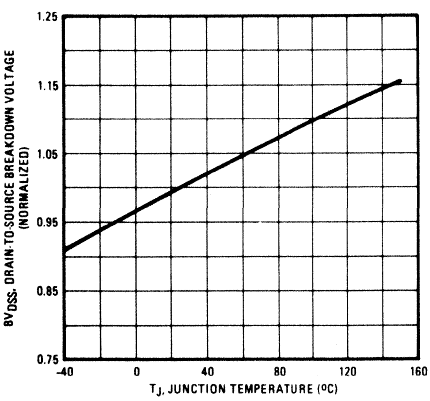


Fig. 9 — Normalized On-Resistance Vs. Temperature

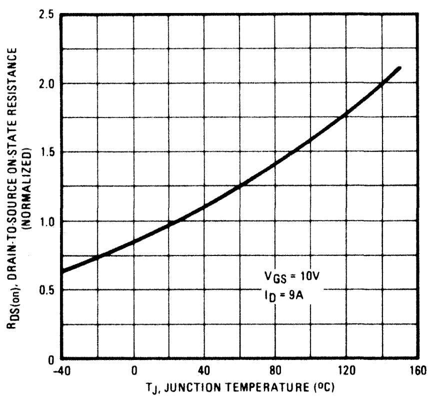


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

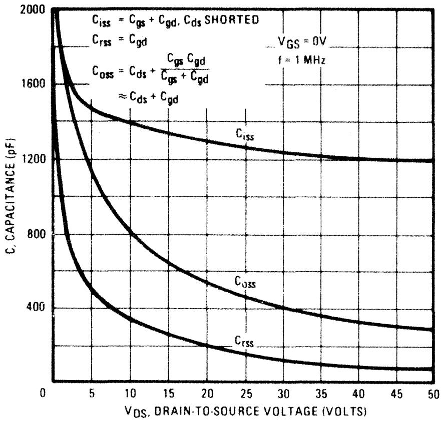


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

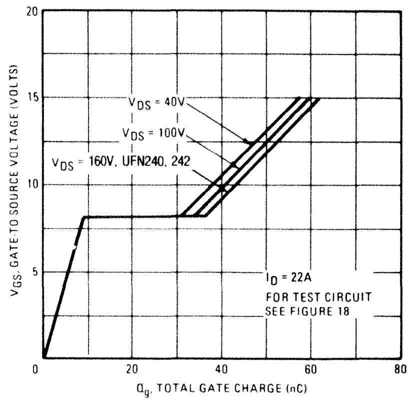


Fig. 12 – Typical On-Resistance Vs. Drain Current

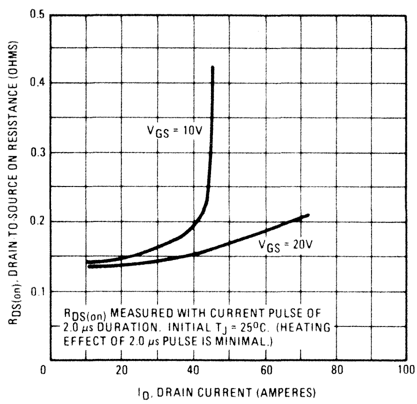


Fig. 13 – Maximum Drain Current Vs. Case Temperature

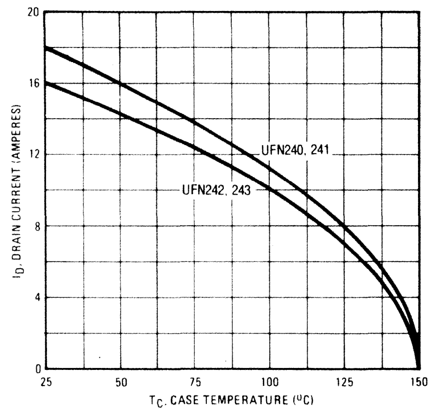


Fig. 14 – Power Vs. Temperature Derating Curve

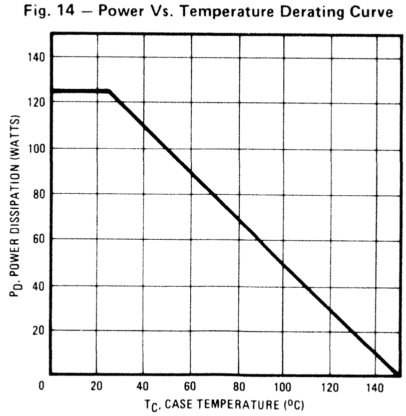


Fig. 15 — Clamped Inductive Test Circuit

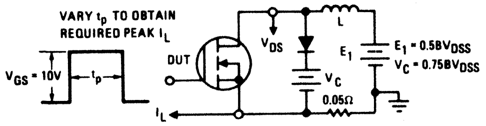


Fig. 16 — Clamped Inductive Waveforms

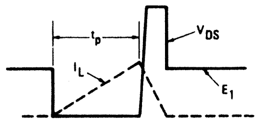


Fig. 17 — Switching Time Test Circuit

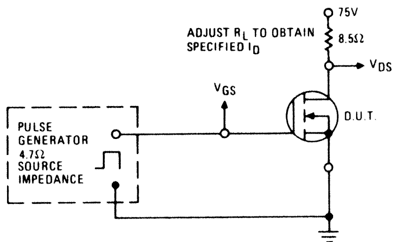
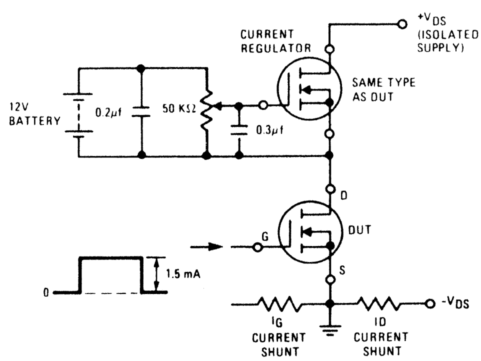


Fig. 18 — Gate Charge Test Circuit



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POWER MOSFET TRANSISTORS

200 Volt, 0.085 Ohm
N-Channel

UFN250
UFN251
UFN252
UFN253

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

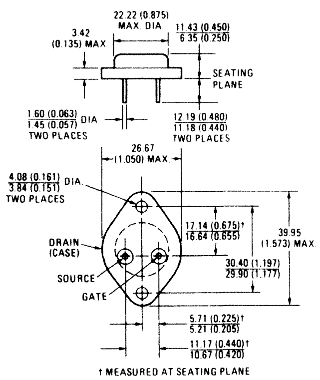
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN250	200V	0.085Ω	30A
UFN251	150V	0.085Ω	30A
UFN252	200V	0.120Ω	25A
UFN253	150V	0.120Ω	25A

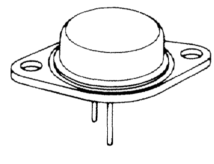
MECHANICAL SPECIFICATIONS

UFN250 UFN251 UFN252 UFN253



Dimensions in Millimeters and (Inches)

TO-3 (Modified)

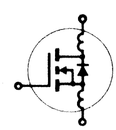


UNITRODE

ABSOLUTE MAXIMUM RATINGS

	Parameter	UFN250	UFN251	UFN252	UFN253	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	30	30	25	25	A
I_D @ T_C = 100°C	Continuous Drain Current	19	19	16	16	A
I_{DM}	Pulsed Drain Current ③	120	120	100	100	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	150 (See Fig. 14)				W
	Linear Derating Factor	1.2 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 120	120	100	100	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

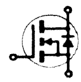
ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFN250 UFN252	200	–	–	V	V_{GS} = 0V
		UFN251 UFN253	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFN250 UFN251	30	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		UFN252 UFN253	25	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFN250 UFN251	–	0.07	0.085	Ω	V_{GS} = 10V, I_D = 16A
		UFN252 UFN253	–	0.09	0.120	Ω	
g_{fs}	Forward Transconductance ②	ALL	8.0	14	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 16A
C_{iss}	Input Capacitance	ALL	–	2000	3000	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	800	1200	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	300	500	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	35	ns	V_{DD} = 95V, I_D = 16A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	100	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	125	ns	
t_f	Fall Time	ALL	–	–	100	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	79	120	nC	V_{GS} = 10V, I_D = 38A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	37	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	42	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die. / Modified MOSFET symbol showing the internal device inductances.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad. 

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	0.83	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	UFN250 UFN251	—	—	30	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFN252 UFN253	—	—	25	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN250 UFN251	—	—	120	A	
		UFN252 UFN253	—	—	100	A	
V_{SD}	Diode Forward Voltage ②	UFN250 UFN251	—	—	2.0	V	$T_C = 25°C, I_S = 30A, V_{GS} = 0V$
		UFN252 UFN253	—	—	1.8	V	$T_C = 25°C, I_S = 25A, V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	750	—	ns	$T_J = 150°C, I_F = 30A, dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	4.7	—	μC	$T_J = 150°C, I_F = 30A, dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25°C$ to $150°C$. ② Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

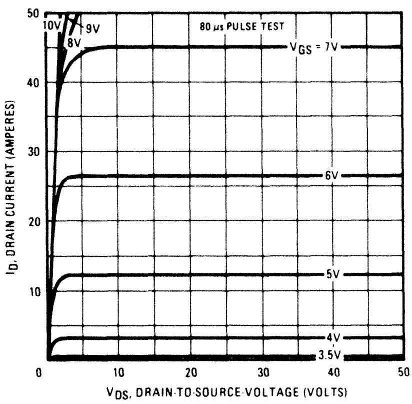


Fig. 2 — Typical Transfer Characteristics

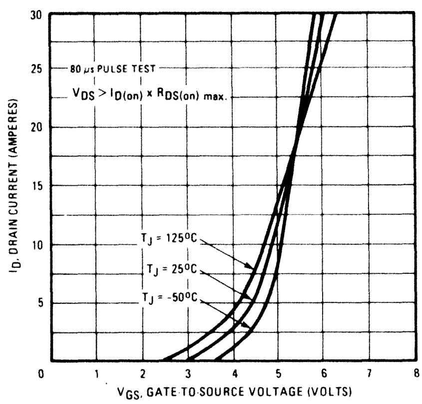


Fig. 3 — Typical Saturation Characteristics

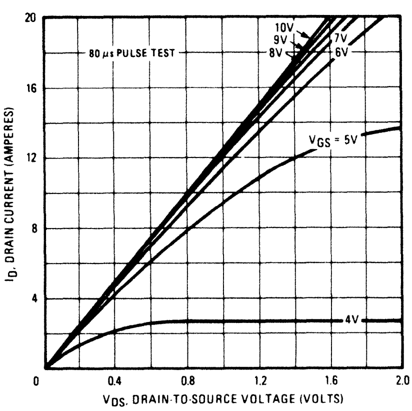


Fig. 4 — Maximum Safe Operating Area

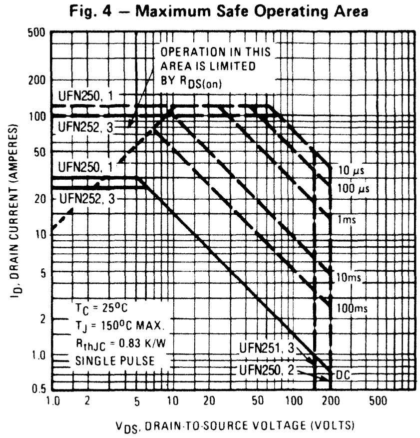


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

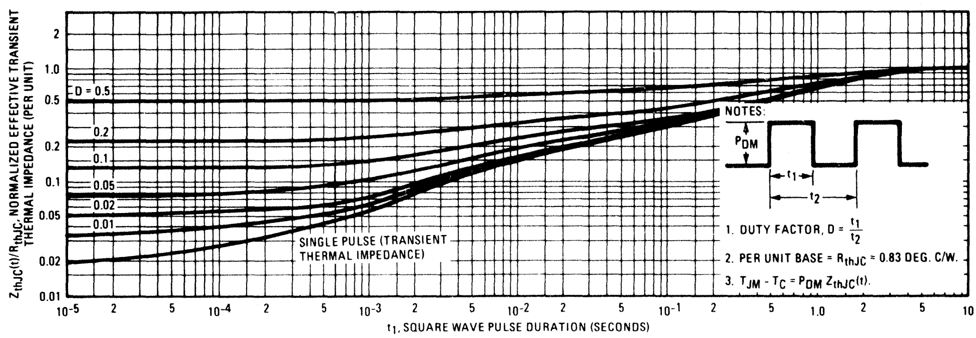


Fig. 6 — Typical Transconductance Vs. Drain Current

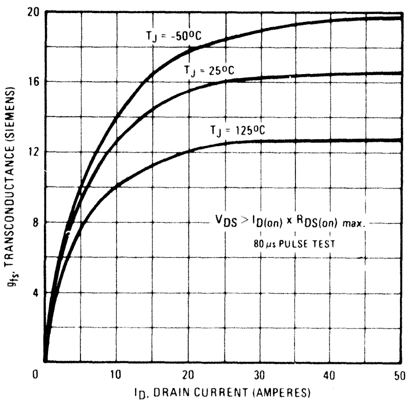


Fig. 7 — Typical Source-Drain Diode Forward Voltage

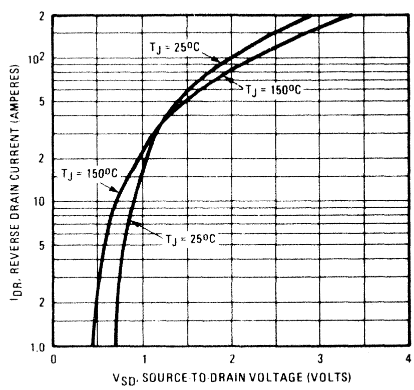


Fig. 8 — Breakdown Voltage Vs. Temperature

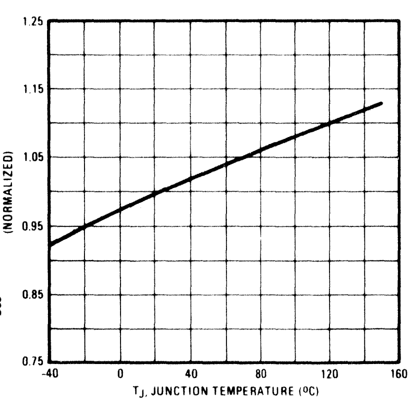


Fig. 9 — Normalized On-Resistance Vs. Temperature

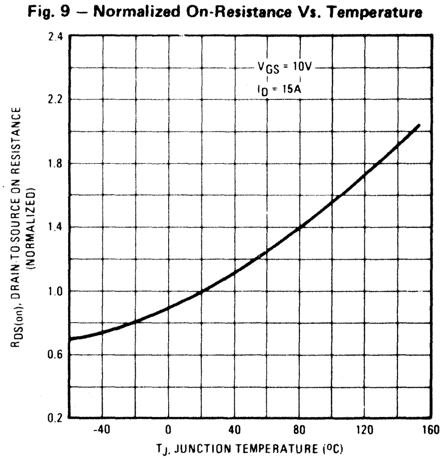


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

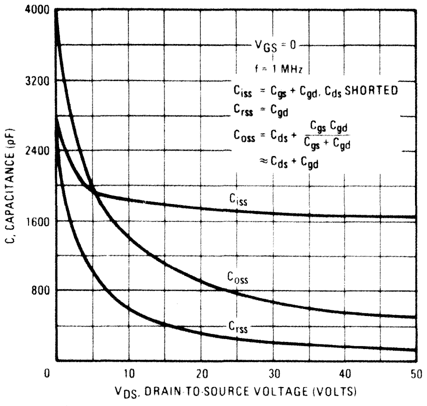


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

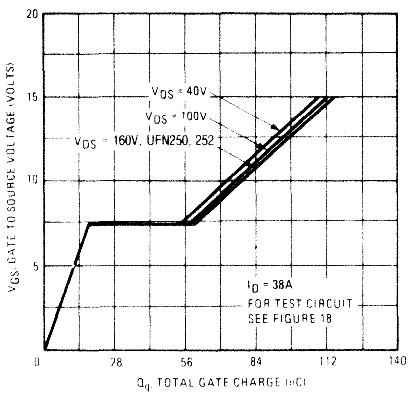


Fig. 12 – Typical On-Resistance Vs. Drain Current

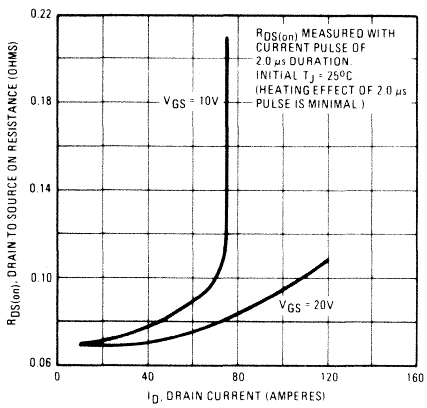


Fig. 13 – Maximum Drain Current Vs. Case Temperature

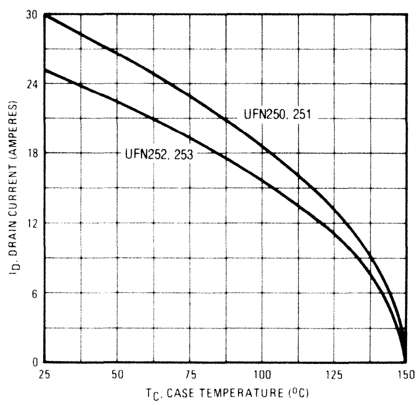


Fig. 14 – Power Vs. Temperature Derating Curve

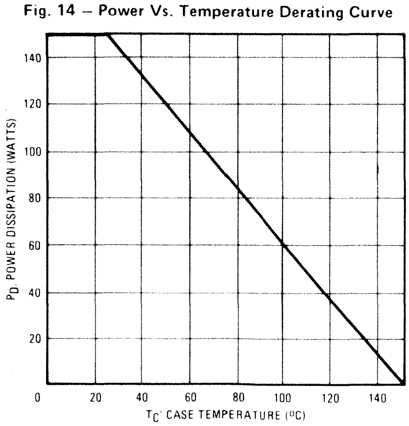


Fig. 15 — Clamped Inductive Test Circuit

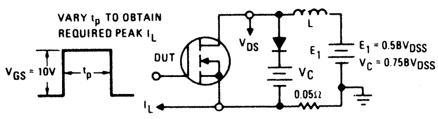


Fig. 16 — Clamped Inductive Waveforms

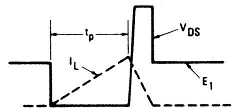


Fig. 17 — Switching Time Test Circuit

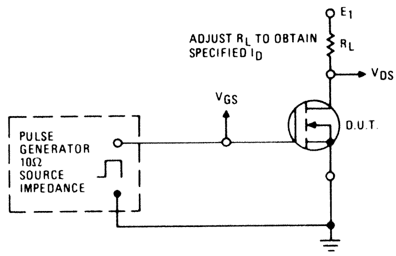
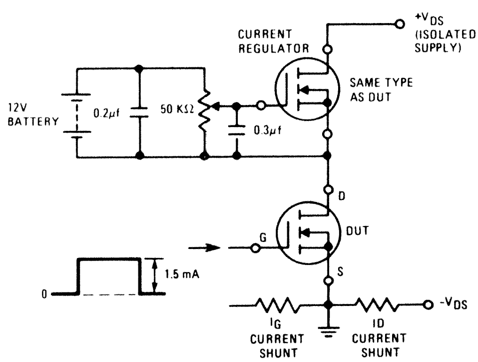


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS
400 Volt, 1.8 Ohm
N-Channel

UFN320
UFN321
UFN322
UFN323

FEATURES
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

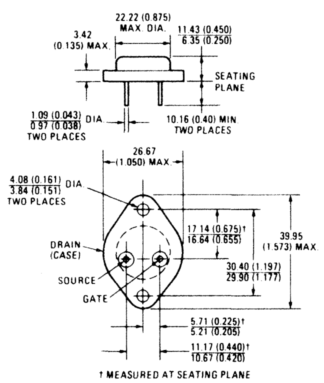
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN320	400V	1.8Ω	3.0A
UFN321	350V	1.8Ω	3.0A
UFN322	400V	2.5Ω	2.5A
UFN323	350V	2.5Ω	2.5A

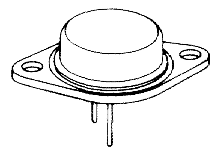
MECHANICAL SPECIFICATIONS

UFN320 UFN321 UFN322 UFN323



Dimensions in Millimeters and (Inches)

TO-3

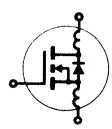


UNITRODE

ABSOLUTE MAXIMUM RATINGS

Parameter		UFN320	UFN321	UFN322	UFN323	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_D @ T_C = 100°C	Continuous Drain Current	2.0	2.0	1.5	1.5	A
I_{DM}	Pulsed Drain Current ③	12	12	10	10	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 12	12	10	10	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

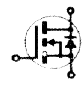
ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFN320 UFN322	400	–	–	V	V_{GS} = 0V
		UFN321 UFN323	350	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFN320 UFN321	3.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		UFN322 UFN323	2.5	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFN320 UFN321	–	1.5	1.8	Ω	V_{GS} = 10V, I_D = 1.5A
		UFN322 UFN323	–	1.8	2.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	2.0	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 1.5A
C_{iss}	Input Capacitance	ALL	–	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	100	200	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	20	40	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 1.5A, Z_0 = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	25	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	25	50	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate Drain)	ALL	–	12	15	nC	V_{GS} = 10V, I_D = 4.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	6.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	6.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die. / Modified MOSFET symbol showing the internal device inductances.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad. 

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN320 UFN321	—	—	3.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFN322 UFN323	—	—	2.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN320 UFN321	—	—	12	A	
		UFN322 UFN323	—	—	10	A	
V_{SD}	Diode Forward Voltage ②	UFN320 UFN321	—	—	1.6	V	$T_C = 25°C$, $I_S = 3.0A$, $V_{GS} = 0V$
		UFN322 UFN323	—	—	1.5	V	$T_C = 25°C$, $I_S = 2.5A$, $V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	450	—	ns	$T_J = 150°C$, $I_F = 3.0A$, $dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	3.1	—	μC	$T_J = 150°C$, $I_F = 3.0A$, $dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25°C$ to $150°C$. ② Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$ ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

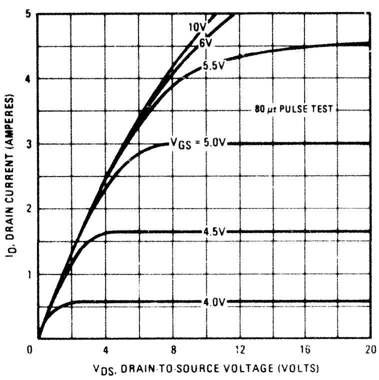


Fig. 2 — Typical Transfer Characteristics

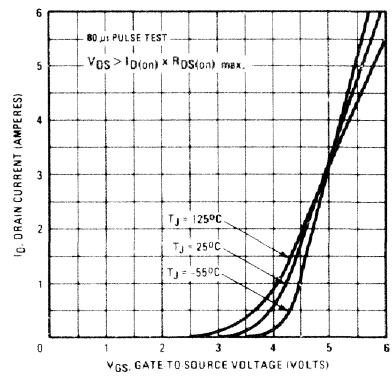


Fig. 3 — Typical Saturation Characteristics

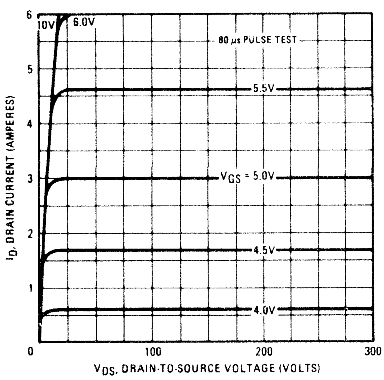
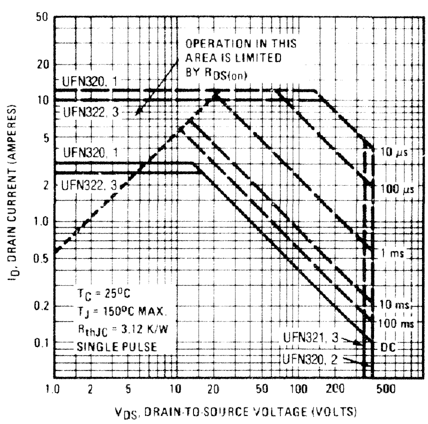


Fig. 4 — Maximum Safe Operating Area



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TWX (710) 326-6509 • TELEX 95-1064

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Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

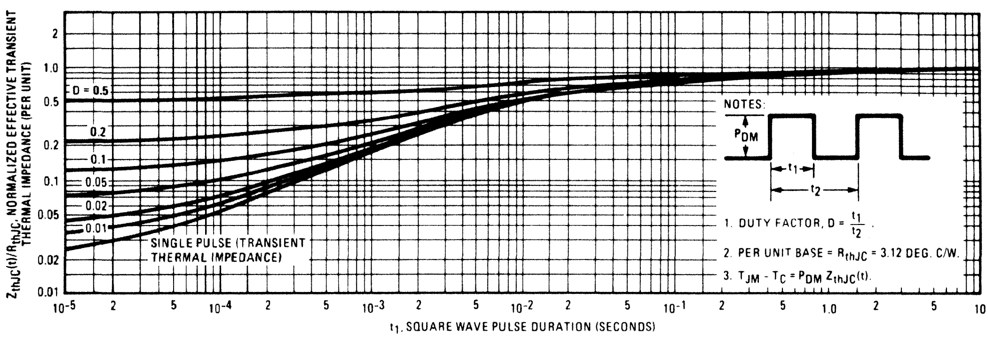


Fig. 6 — Typical Transconductance Vs. Drain Current

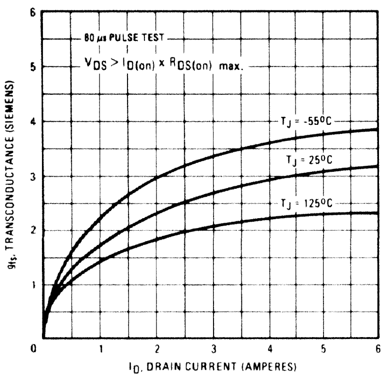


Fig. 7 — Typical Source-Drain Diode Forward Voltage

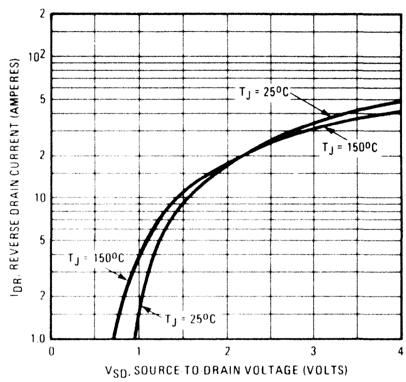


Fig. 8 — Breakdown Voltage Vs. Temperature

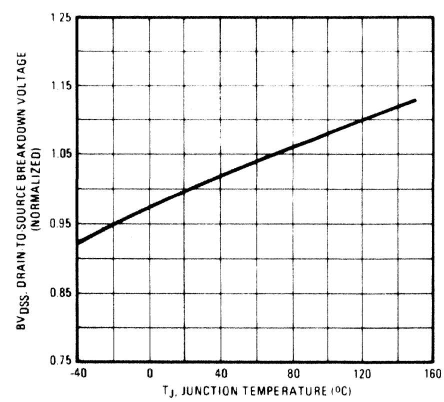


Fig. 9 — Normalized On-Resistance Vs. Temperature

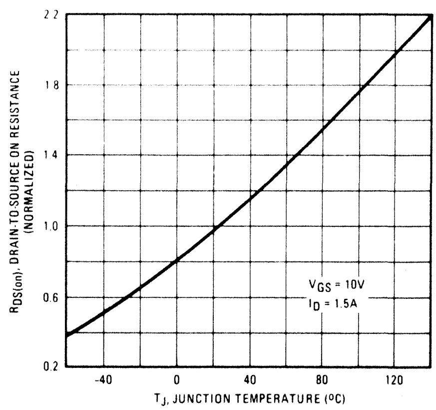


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

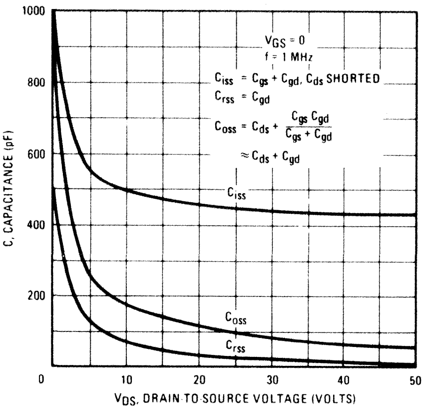


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

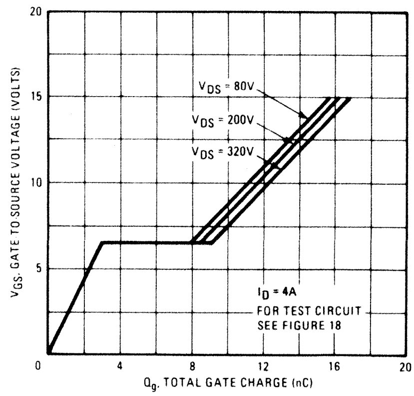


Fig. 12 — Typical On-Resistance Vs. Drain Current

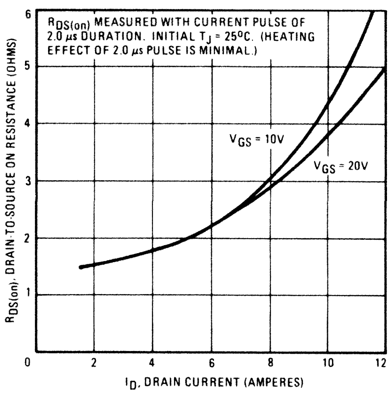


Fig. 13 — Maximum Drain Current Vs. Case Temperature

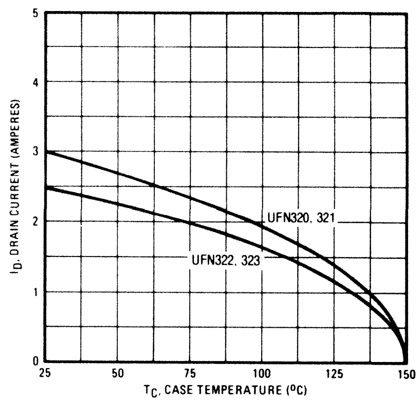


Fig. 14 — Power Vs. Temperature Derating Curve

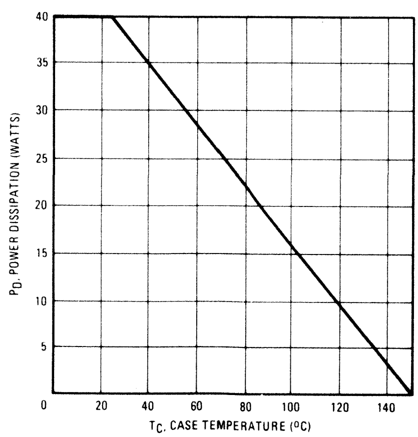


Fig. 15 — Clamped Inductive Test Circuit

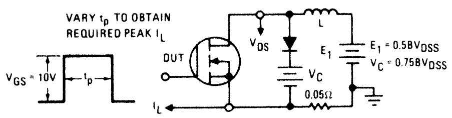


Fig. 16 — Clamped Inductive Waveforms

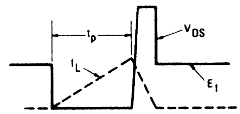


Fig. 17 — Switching Time Test Circuit

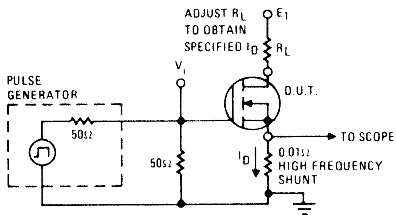
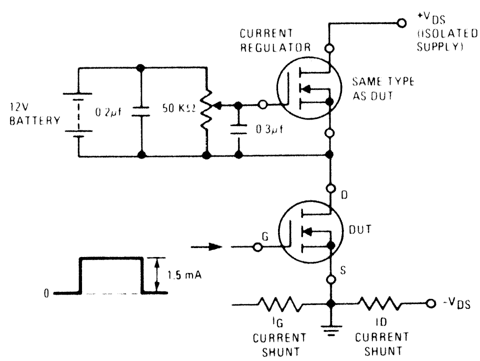


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

400 Volt, 1.0 Ohm
N-Channel

UFN330
UFN331
UFN332
UFN333

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

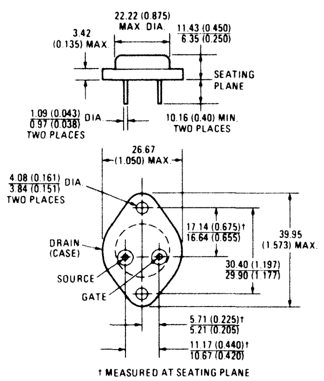
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN330	400V	1.0Ω	5.5A
UFN331	350V	1.0Ω	5.5A
UFN332	400V	1.5Ω	4.5A
UFN333	350V	1.5Ω	4.5A

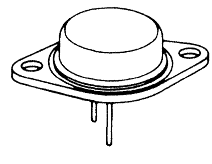
MECHANICAL SPECIFICATIONS

UFN330 UFN331 UFN332 UFN333



Dimensions in Millimeters and (Inches)

TO-3



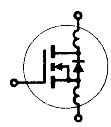
4/83

UNITRODE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	UFN330	UFN331	UFN332	UFN333	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	5.5	5.5	4.5	4.5	A
I_D @ T_C = 100°C	Continuous Drain Current	3.5	3.5	3.0	3.0	A
I_{DM}	Pulsed Drain Current ③	22	22	18	18	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 22	22	18	18	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

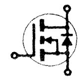
ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Symbol	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFN330 UFN332	400	–	–	V	V_{GS} = 0V I_D = 250μA
		UFN331 UFN333	350	–	–	V	
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFN330 UFN331	5.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		UFN332 UFN333	4.5	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFN330 UFN331	–	0.8	1.0	Ω	V_{GS} = 10V, I_D = 3.0A
		UFN332 UFN333	–	1.0	1.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	3.0	4.0	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 3.0A
C_{iss}	Input Capacitance	ALL	–	700	900	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	150	300	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	40	80	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} = 175V, I_D = 3.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	35	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	55	ns	
t_f	Fall Time	ALL	–	–	35	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	18	30	nC	V_{GS} = 10V, I_D = 7.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	11	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	7.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die. / Modified MOSFET symbol showing the internal device inductances. 
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

THERMAL RESISTANCE

Symbol	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
R_{thJC}	Junction-to-Case	ALL	–	–	1.67	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN330 UFN331	–	–	5.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFN332 UFN333	–	–	4.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN330 UFN331	–	–	22	A	
		UFN332 UFN333	–	–	18	A	
V_{SD}	Diode Forward Voltage ②	UFN330 UFN331	–	–	1.6	V	T_C = 25°C, I_S = 5.5A, V_{GS} = 0V
		UFN332 UFN333	–	–	1.5	V	T_C = 25°C, I_S = 4.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	600	–	ns	T_J = 150°C, I_F = 5.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.0	–	μC	T_J = 150°C, I_F = 5.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

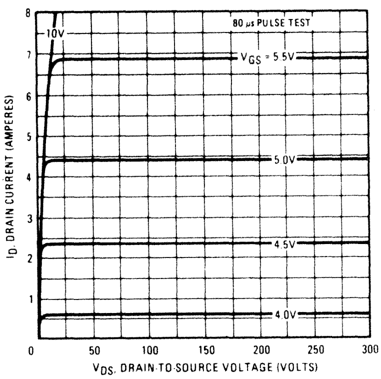


Fig. 2 — Typical Transfer Characteristics

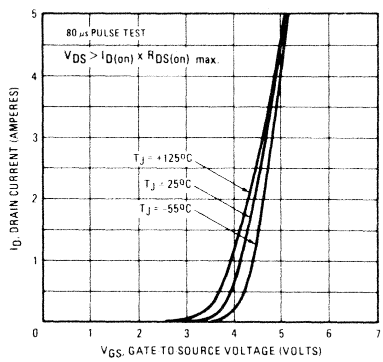


Fig. 3 — Typical Saturation Characteristics

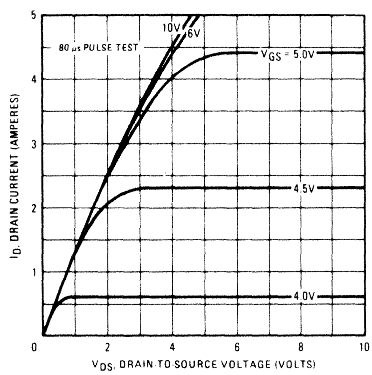


Fig. 4 — Maximum Safe Operating Area

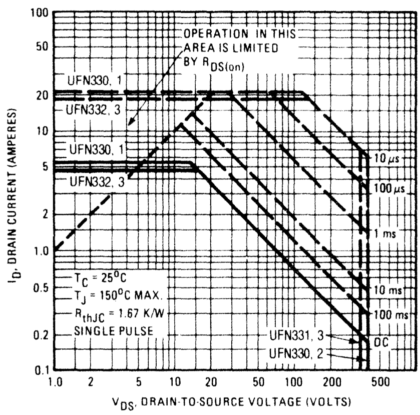


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

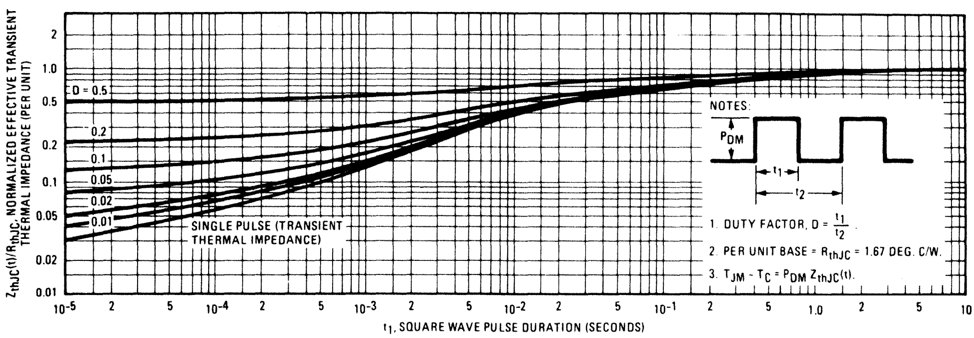


Fig. 6 — Typical Transconductance Vs. Drain Current

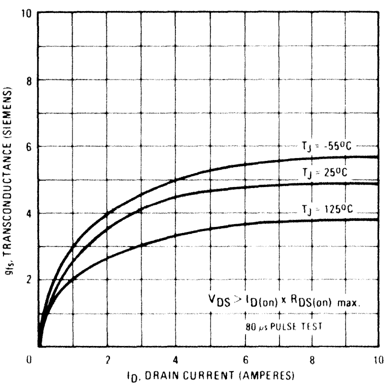


Fig. 7 — Typical Source-Drain Diode Forward Voltage

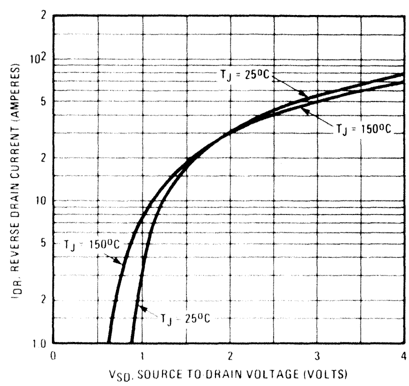


Fig. 8 — Breakdown Voltage Vs. Temperature

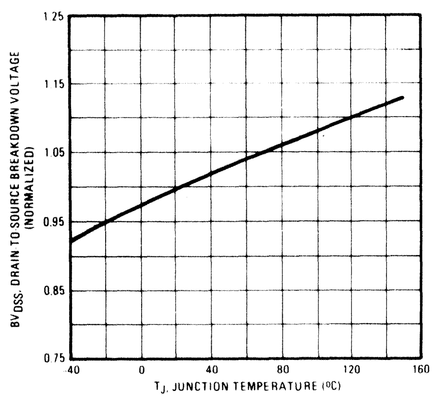


Fig. 9 — Normalized On-Resistance Vs. Temperature

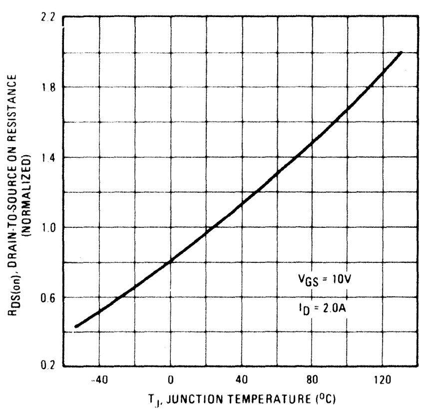


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

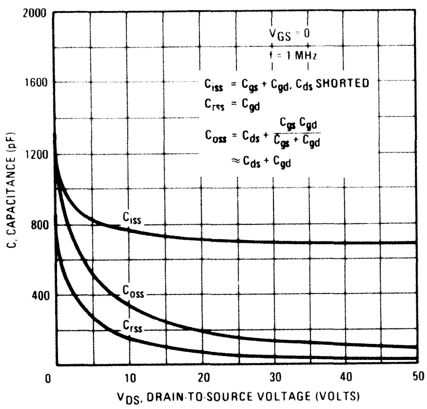


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

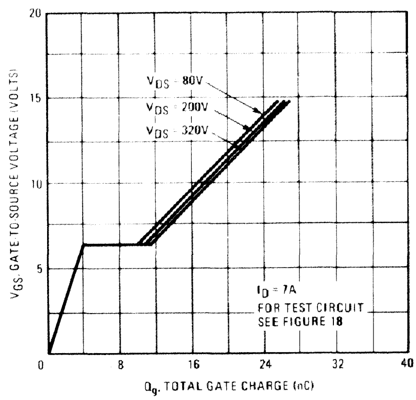


Fig. 12 – Typical On-Resistance Vs. Drain Current

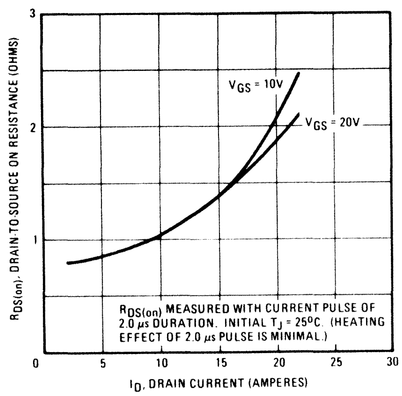


Fig. 13 – Maximum Drain Current Vs. Case Temperature

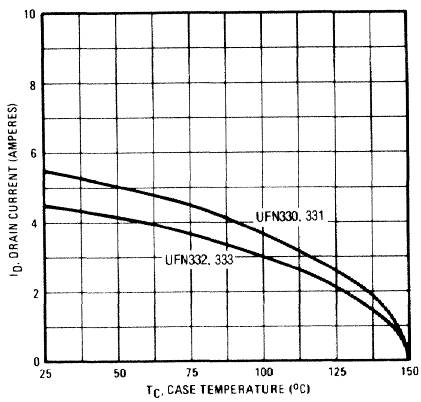


Fig. 14 – Power Vs. Temperature Derating Curve

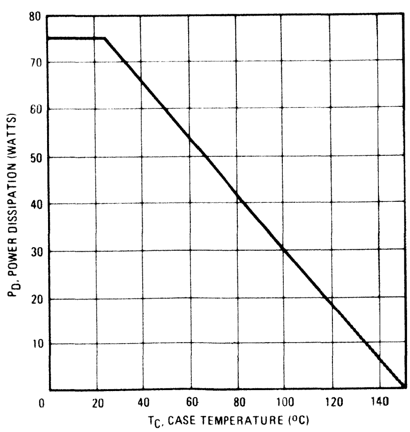


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Fig. 15 – Clamped Inductive Test Circuit

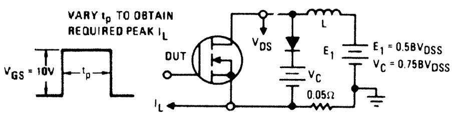


Fig. 16 – Clamped Inductive Waveforms

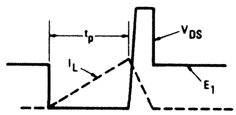


Fig. 17 – Switching Time Test Circuit

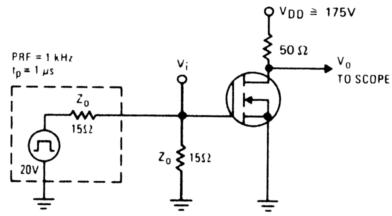
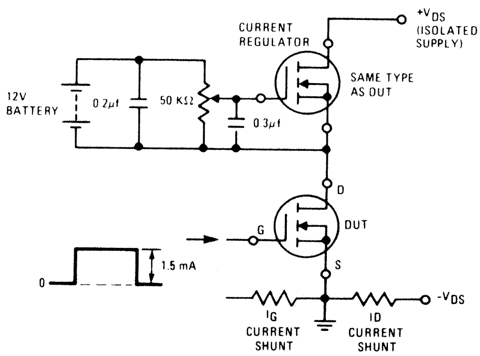


Fig. 18 – Gate Charge Test Circuit



POWER MOSFET TRANSISTORS
400 Volt, 0.55 Ohm
N-Channel

UFN340
UFN341
UFN342
UFN343

FEATURES
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION
The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

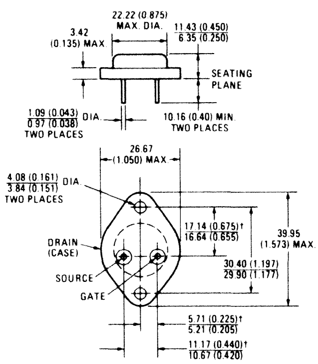
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN340	400V	0.55Ω	10A
UFN341	350V	0.55Ω	10A
UFN342	400V	0.80Ω	8.0A
UFN343	350V	0.80Ω	8.0A

MECHANICAL SPECIFICATIONS

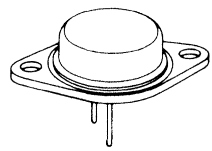
UFN340 UFN341 UFN342 UFN343



† MEASURED AT SEATING PLANE

Dimensions in Millimeters and (Inches)

TO-3

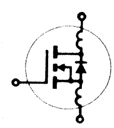


UNITRODE

ABSOLUTE MAXIMUM RATINGS

Parameter		UFN340	UFN341	UFN342	UFN343	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	10	10	8.0	8.0	A
I_D @ T_C = 100°C	Continuous Drain Current	6.0	6.0	5.0	5.0	A
I_{DM}	Pulsed Drain Current ③	40	40	32	32	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 40	40	32	32	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

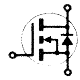
ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFN340 UFN342	400	—	—	V	V_{GS} = 0V
		UFN341 UFN343	350	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFN340 UFN341	10	—	—	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		UFN342 UFN343	8.0	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFN340 UFN341	—	0.47	0.55	Ω	V_{GS} = 10V, I_D = 5.0A
		UFN342 UFN343	—	0.68	0.80	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	7.0	—	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 5.0A
C_{iss}	Input Capacitance	ALL	—	1250	1600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	300	450	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	80	150	pF	
$t_{d(on)}$	Turn On Delay Time	ALL	—	17	35	ns	V_{DD} = 175V, I_D = 5.0A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	5.0	15	ns	
$t_{d(off)}$	Turn Off Delay Time	ALL	—	45	90	ns	
t_f	Fall Time	ALL	—	16	35	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	41	60	nC	V_{GS} = 10V, I_D = 12A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	18	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	23	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die. / Modified MOSFET symbol showing the internal device inductances.
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad. 

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	—	—	1.0	K/W	
R_{thCS}	Case-to-Sink	ALL	—	0.1	—	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN340 UFN341	—	—	10	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFN342 UFN343	—	—	8.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN340 UFN341	—	—	40	A	
		UFN342 UFN343	—	—	32	A	
V_{SD}	Diode Forward Voltage ②	UFN340 UFN341	—	—	2.0	V	$T_C = 25°C, I_S = 10A, V_{GS} = 0V$
		UFN342 UFN343	—	—	1.9	V	$T_C = 25°C, I_S = 8.0A, V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	800	—	ns	$T_J = 150°C, I_F = 10A, dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	5.7	—	μC	$T_J = 150°C, I_F = 10A, dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25°C$ to $150°C$. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

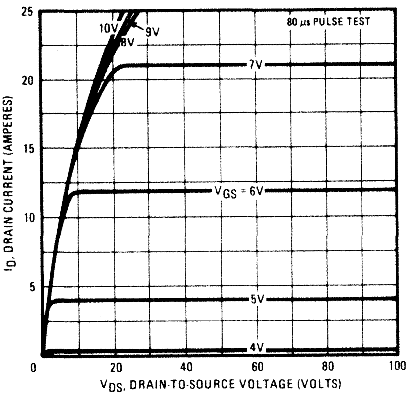


Fig. 2 — Typical Transfer Characteristics

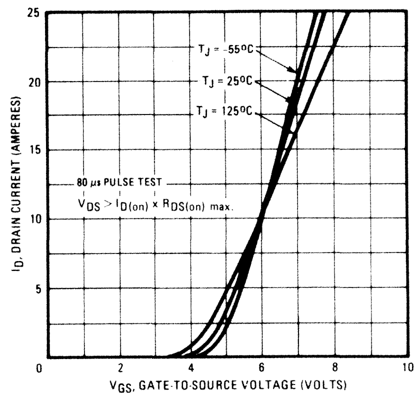


Fig. 3 — Typical Saturation Characteristics

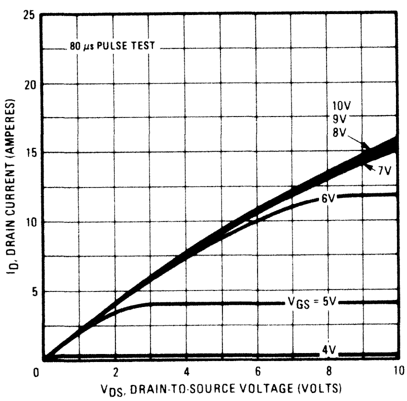


Fig. 4 — Maximum Safe Operating Area

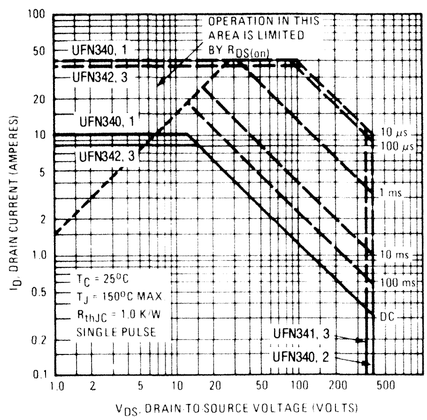


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

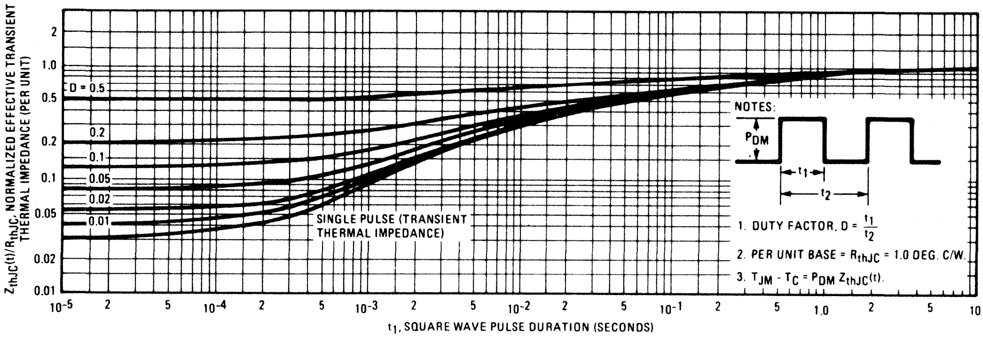


Fig. 6 — Typical Transconductance Vs. Drain Current

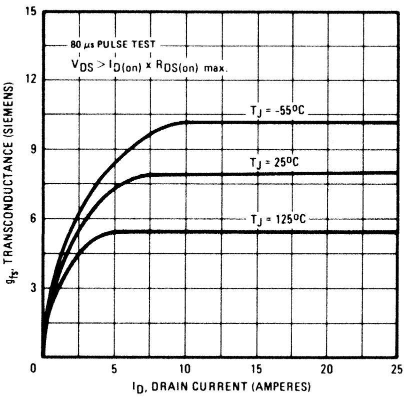


Fig. 7 — Typical Source-Drain Diode Forward Voltage

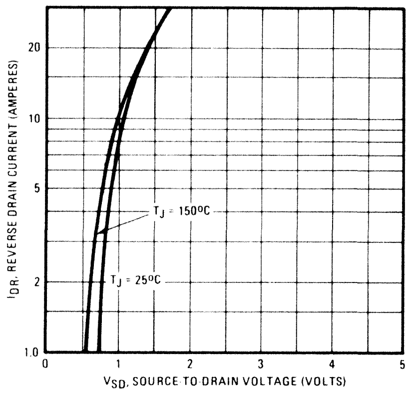


Fig. 8 — Breakdown Voltage Vs. Temperature

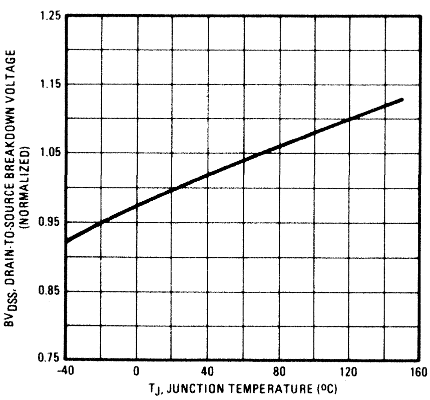


Fig. 9 — Normalized On-Resistance Vs. Temperature

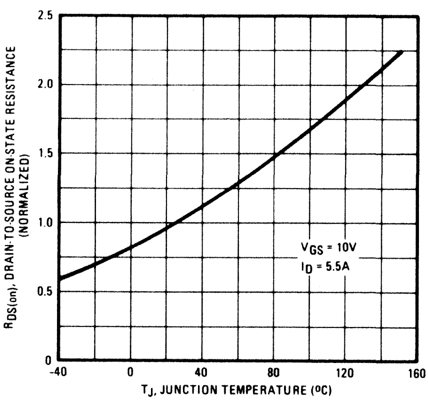


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

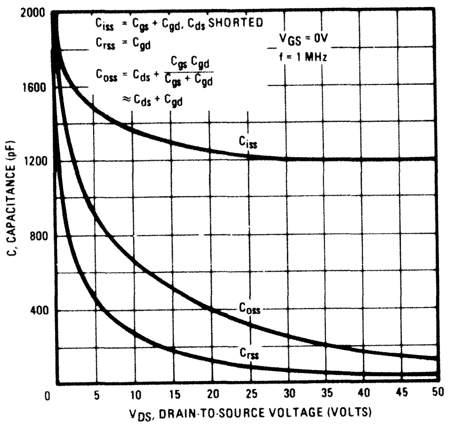


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

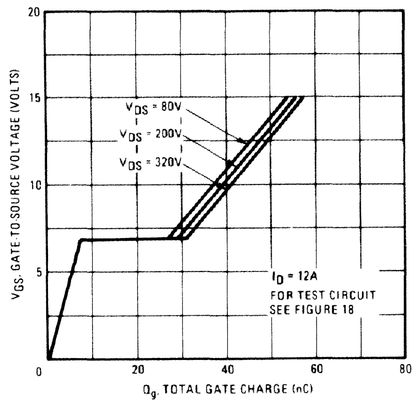


Fig. 12 – Typical On-Resistance Vs. Drain Current

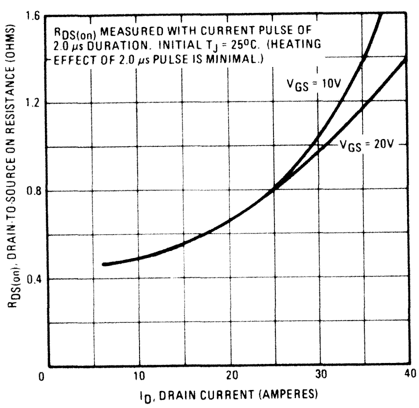


Fig. 13 – Maximum Drain Current Vs. Case Temperature

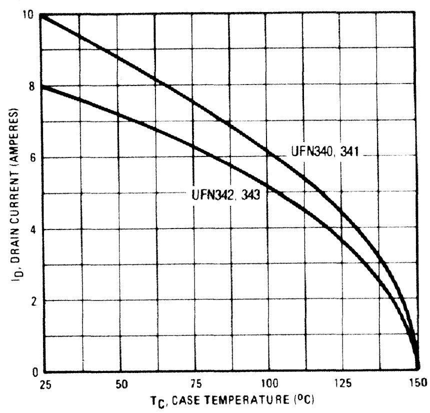


Fig. 14 – Power Vs. Temperature Derating Curve

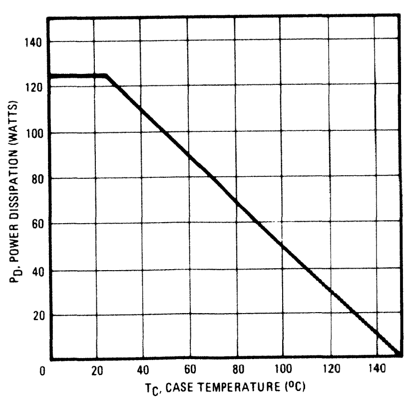


Fig. 15 – Clamped Inductive Test Circuit

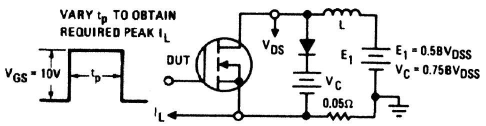


Fig. 16 – Clamped Inductive Waveforms

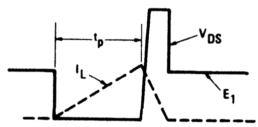


Fig. 17 – Switching Time Test Circuit

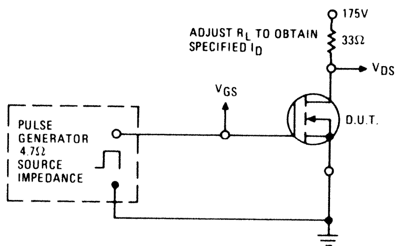
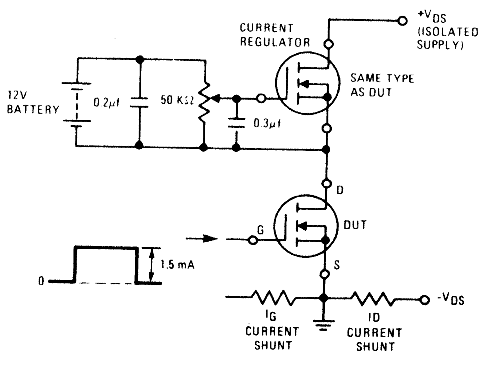


Fig. 18 – Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

400 Volt, 0.3 Ohm
N-Channel

UFN350
UFN351
UFN352
UFN353

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

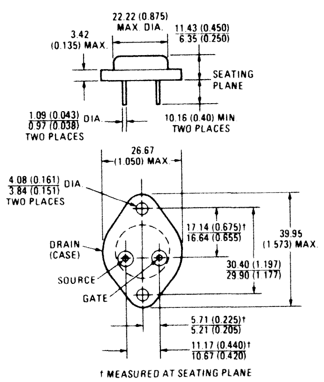
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN350	400V	0.3Ω	15A
UFN351	350V	0.3Ω	15A
UFN352	400V	0.4Ω	13A
UFN353	350V	0.4Ω	13A

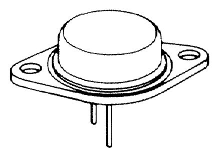
MECHANICAL SPECIFICATIONS

UFN350 UFN351 UFN352 UFN353



Dimensions in Millimeters and (Inches)

TO-3

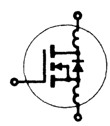


UNITRODE

ABSOLUTE MAXIMUM RATINGS

	Parameter	UFN350	UFN351	UFN352	UFN353	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	15	15	13	13	A
I_D @ T_C = 100°C	Continuous Drain Current	9.0	9.0	8.0	8.0	A
I_{DM}	Pulsed Drain Current ③	60	60	52	52	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	150 (See Fig. 14)				W
	Linear Derating Factor	1.2 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 60	60	52	52	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

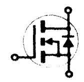
ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFN350 UFN352	400	–	–	V	V_{GS} = 0V
		UFN351 UFN353	350	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	−100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFN350 UFN351	15	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\,max.}$, V_{GS} = 10V
		UFN352 UFN353	13	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFN350 UFN351	–	0.25	0.3	Ω	V_{GS} = 10V, I_D = 8.0A
		UFN352 UFN353	–	0.3	0.4	Ω	
g_{fs}	Forward Transconductance ②	ALL	8.0	10	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)\,max.}$, I_D = 8.0A
C_{iss}	Input Capacitance	ALL	–	2000	3000	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	400	600	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	100	200	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	35	ns	V_{DD} ≈ 180V, I_D = 8.0A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	65	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	150	ns	
t_f	Fall Time	ALL	–	–	75	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	79	120	nC	V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	38	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	41	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die. — Modified MOSFET symbol showing the internal device inductances. 
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	0.83	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN350 UFN351	—	—	15	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFN352 UFN353	—	—	13	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN350 UFN351	—	—	60	A	
		UFN352 UFN353	—	—	52	A	
V_{SD}	Diode Forward Voltage ②	UFN350 UFN351	—	—	1.6	V	$T_C = 25°C, I_S = 15A, V_{GS} = 0V$
		UFN352 UFN353	—	—	1.5	V	$T_C = 25°C, I_S = 13A, V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	1000	—	ns	$T_J = 150°C, I_F = 15A, dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	6.6	—	μC	$T_J = 150°C, I_F = 15A, dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25°C$ to $150°C$. ② Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

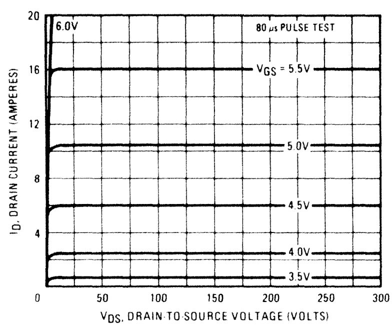


Fig. 2 — Typical Transfer Characteristics

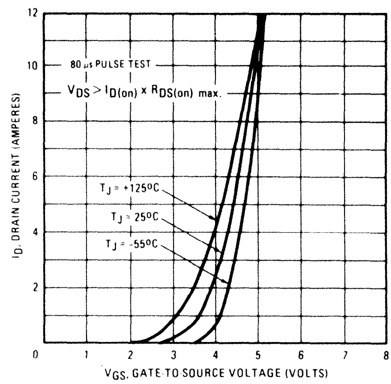


Fig. 3 — Typical Saturation Characteristics

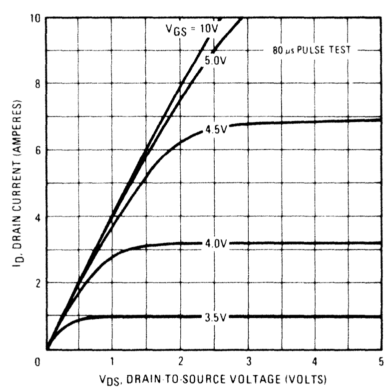


Fig. 4 — Maximum Safe Operating Area

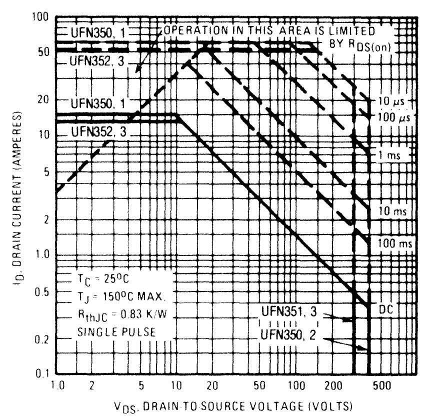


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

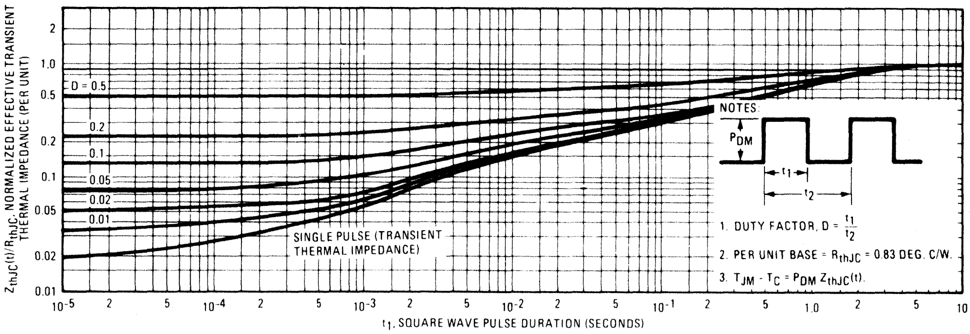


Fig. 6 – Typical Transconductance Vs. Drain Current

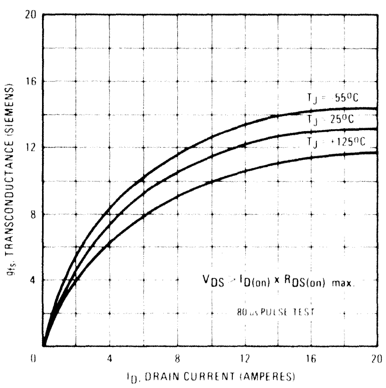


Fig. 7 – Typical Source-Drain Diode Forward Voltage

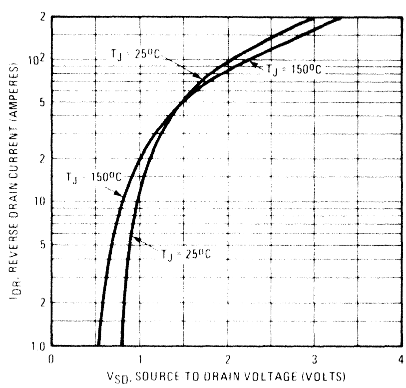


Fig. 8 – Breakdown Voltage Vs. Temperature

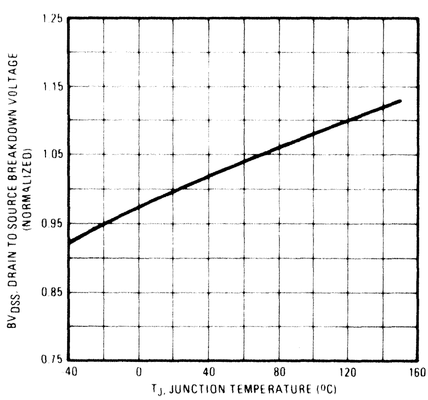


Fig. 9 – Normalized On-Resistance Vs. Temperature

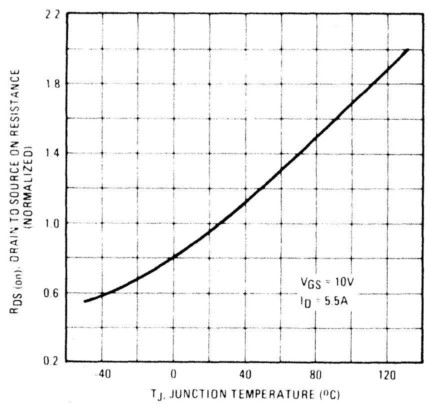


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Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

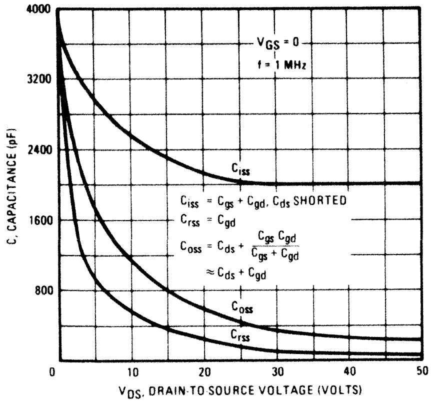


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

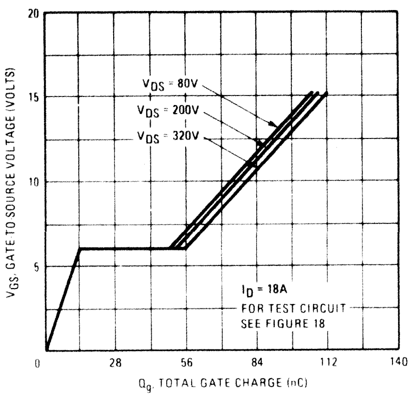


Fig. 12 – Typical On-Resistance Vs. Drain Current

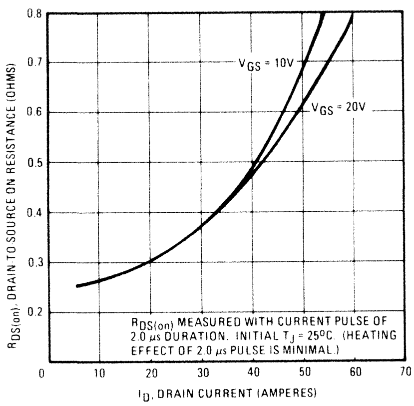


Fig. 13 – Maximum Drain Current Vs. Case Temperature

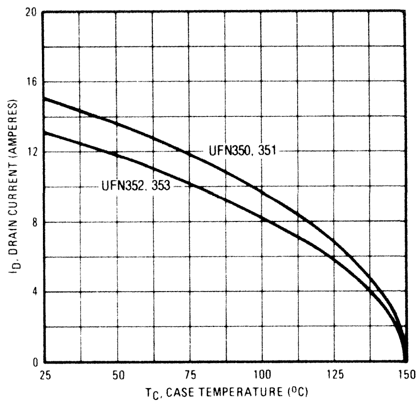


Fig. 14 – Power Vs. Temperature Derating Curve

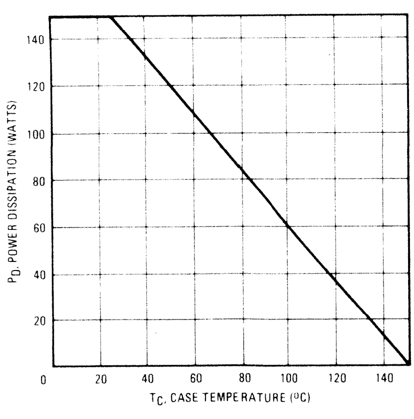


Fig. 15 — Clamped Inductive Test Circuit

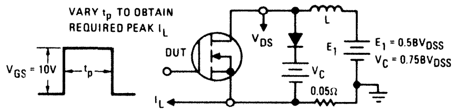


Fig. 16 — Clamped Inductive Waveforms

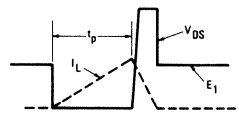


Fig. 17 — Switching Time Test Circuit

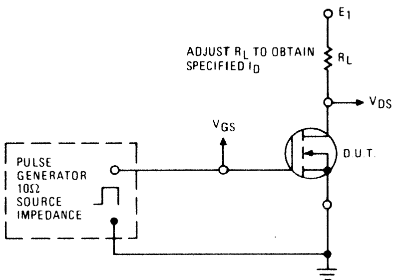
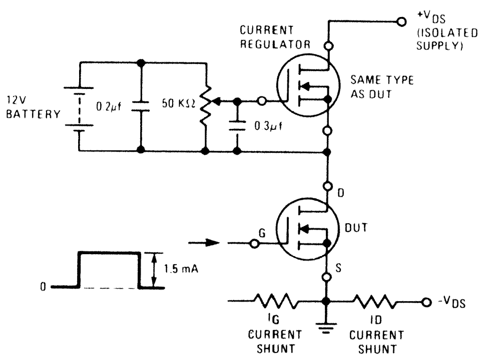


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

500 Volt, 3.0 Ohm
N-Channel

UFN420
UFN421
UFN422
UFN423

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

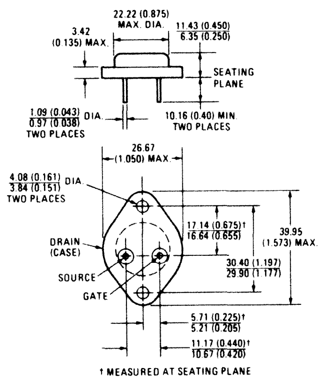
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN420	500V	3.0Ω	2.5A
UFN421	450V	3.0Ω	2.5A
UFN422	500V	4.0Ω	2.0A
UFN423	450V	4.0Ω	2.0A

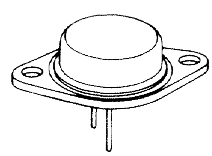
MECHANICAL SPECIFICATIONS

UFN420 UFN421 UFN422 UFN423



Dimensions in Millimeters and (Inches)

TO-3



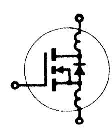
4/83

UNITRODE

ABSOLUTE MAXIMUM RATINGS

Parameter		UFN420	UFN421	UFN422	UFN423	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	2.5	2.5	2.0	2.0	A
I_D @ T_C = 100°C	Continuous Drain Current	1.5	1.5	1.0	1.0	A
I_{DM}	Pulsed Drain Current ③	10	10	8.0	8.0	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 10	10	8.0	8.0	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

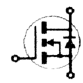
ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFN420 UFN422	500	—	—	V	V_{GS} = 0V
		UFN421 UFN423	450	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFN420 UFN421	2.5			A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		UFN422 UFN423	2.0	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFN420 UFN421	—	2.5	3.0	Ω	V_{GS} = 10V, I_D = 1.0A
		UFN422 UFN423	—	3.0	4.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	1.75	—	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 1.0A
C_{iss}	Input Capacitance	ALL	—	300	400	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	75	150	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	20	40	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	30	60	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 1.0A, Z_O = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	25	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	30	60	ns	
t_f	Fall Time	ALL	—	15	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	11	15	nC	V_{GS} = 10V, I_D = 3.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	5.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	6.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die. Modified MOSFET symbol showing the internal device inductances.
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad. 

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	—	—	3.12	K/W	
R_{thCS}	Case-to-Sink	ALL	—	0.1	—	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN420 UFN421	–	–	2.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFN422 UFN423	–	–	2.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN420 UFN421	–	–	10	A	
		UFN422 UFN423	–	–	8.0	A	
V_{SD}	Diode Forward Voltage ②	UFN420 UFN421	–	–	1.4	V	$T_C = 25°C, I_S = 2.5A, V_{GS} = 0V$
		UFN422 UFN423	–	–	1.3	V	$T_C = 25°C, I_S = 2.0A, V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	–	600	–	ns	$T_J = 150°C, I_F = 2.5A, dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	–	3.5	–	μC	$T_J = 150°C, I_F = 2.5A, dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25°C$ to $150°C$. ② Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

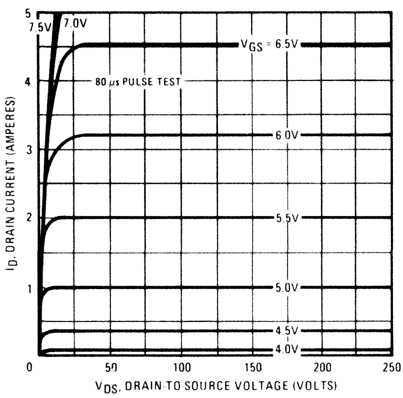


Fig. 2 — Typical Transfer Characteristics

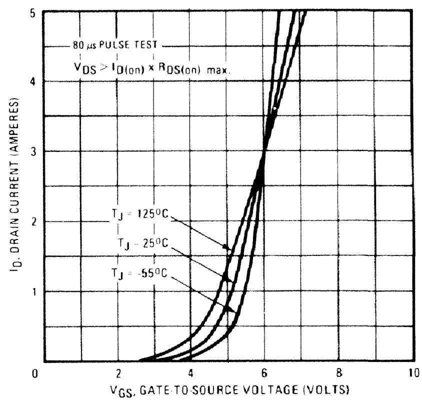


Fig. 3 — Typical Saturation Characteristics

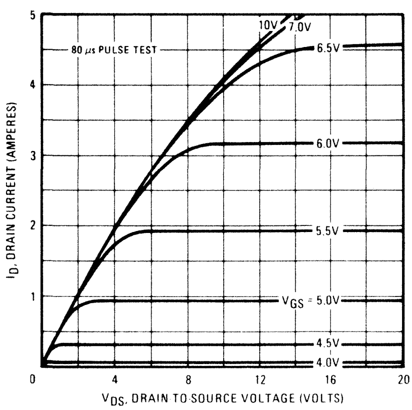


Fig. 4 — Maximum Safe Operating Area

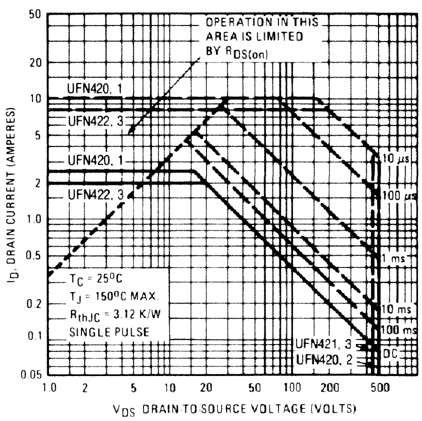


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

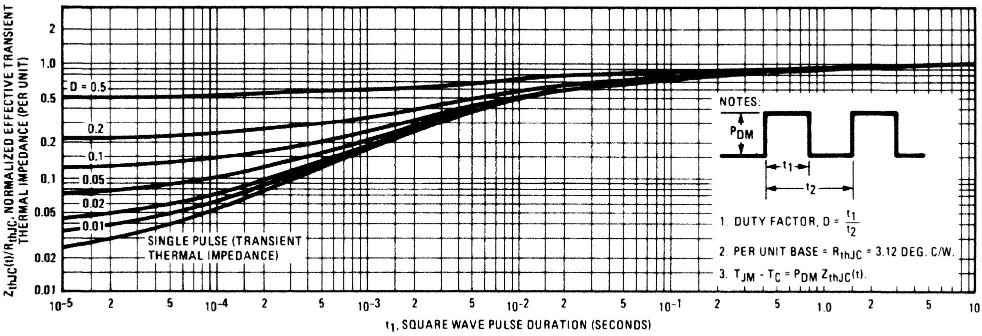


Fig. 6 — Typical Transconductance Vs. Drain Current

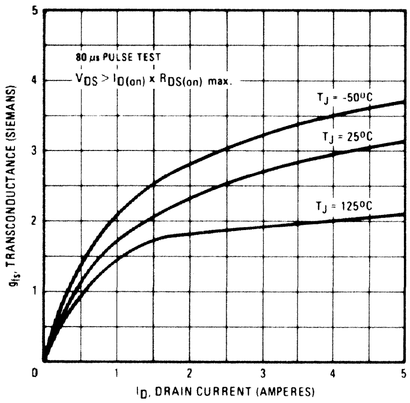


Fig. 7 — Typical Source-Drain Diode Forward Voltage

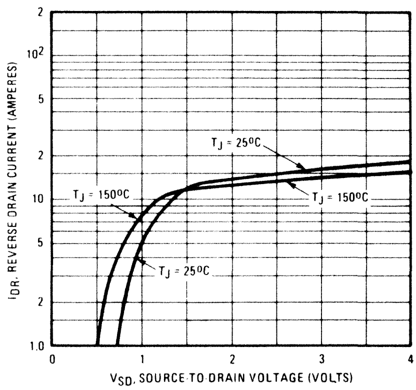


Fig. 8 — Breakdown Voltage Vs. Temperature

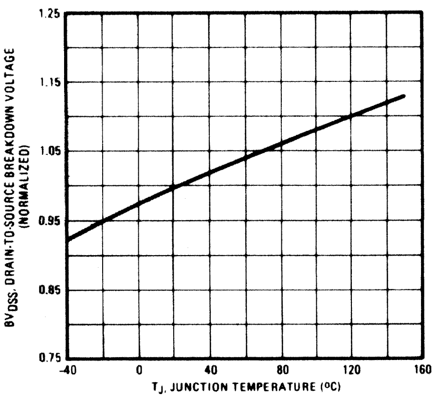


Fig. 9 — Normalized On-Resistance Vs. Temperature

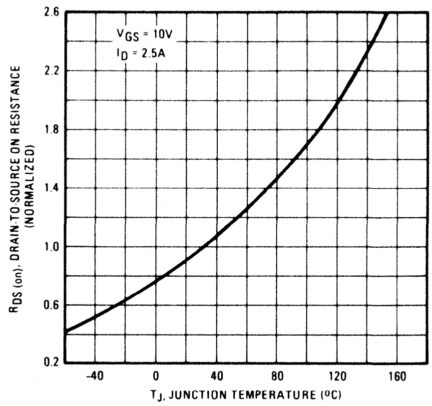


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

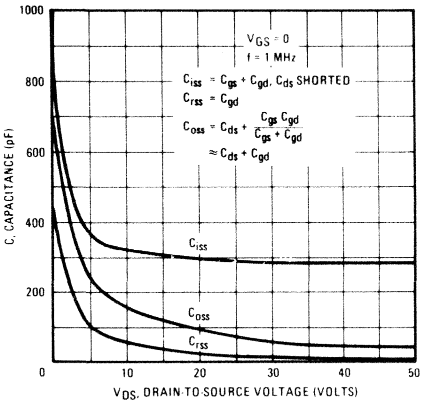


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

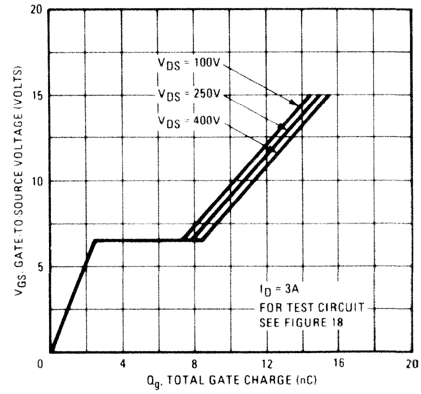


Fig. 12 – Typical On-Resistance Vs. Drain Current

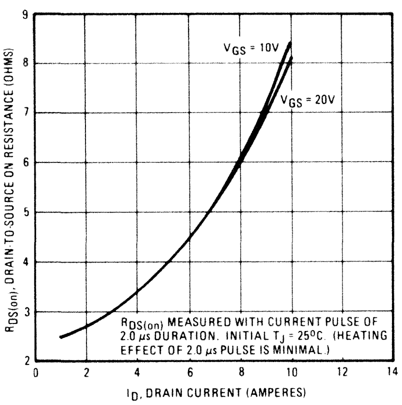


Fig. 13 – Maximum Drain Current Vs. Case Temperature

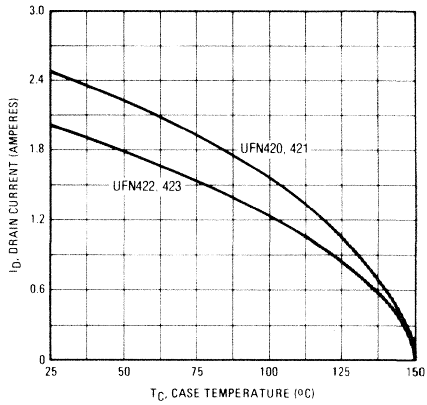


Fig. 14 – Power Vs. Temperature Derating Curve

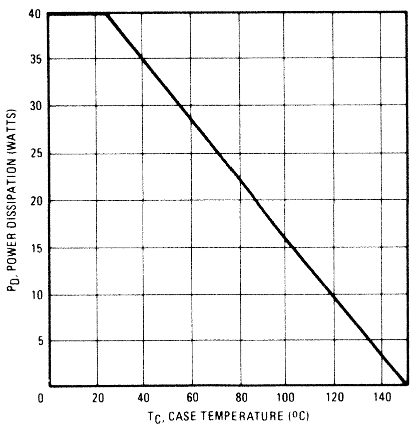


Fig. 15 — Clamped Inductive Test Circuit

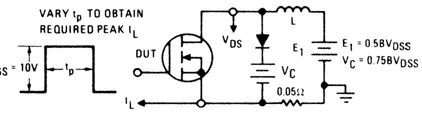


Fig. 16 — Clamped Inductive Waveforms

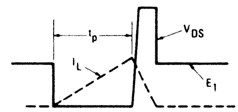


Fig. 17 — Switching Time Test Circuit

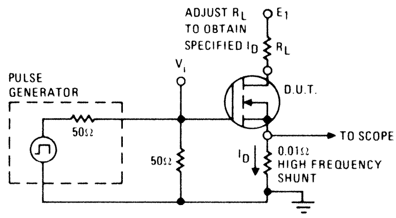
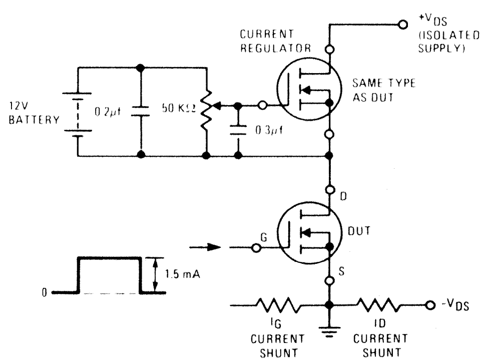


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

500 Volt, 1.5 Ohm
N-Channel

UFN430
UFN431
UFN432
UFN433

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

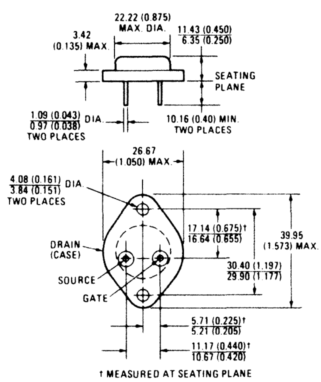
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN430	500V	1.5Ω	4.5A
UFN431	450V	1.5Ω	4.5A
UFN432	500V	2.0Ω	4.0A
UFN433	450V	2.0Ω	4.0A

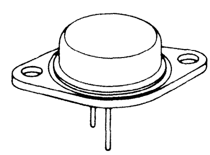
MECHANICAL SPECIFICATIONS

UFN430 UFN431 UFN432 UFN433



Dimensions in Millimeters and (Inches)

TO-3

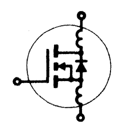


UNITRODE

ABSOLUTE MAXIMUM RATINGS

Parameter		UFN430	UFN431	UFN432	UFN433	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	4.5	4.5	4.0	4.0	A
I_D @ T_C = 100°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_{DM}	Pulsed Drain Current ③	18	18	16	16	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 18	18	16	16	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFN430 UFN432	500	–	–	V	V_{GS} = 0V
		UFN431 UFN433	450	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFN430 UFN431	4.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		UFN432 UFN433	4.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFN430 UFN431	–	1.3	1.5	Ω	V_{GS} = 10V, I_D = 2.5A
		UFN432 UFN433	–	1.5	2.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	2.5	3.2	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 2.5A
C_{iss}	Input Capacitance	ALL	–	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	100	200	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	30	60	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} = 225V, I_D = 2.5A, Z_O = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	30	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	55	ns	
t_f	Fall Time	ALL	–	–	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	22	30	nC	V_{GS} = 10V, I_D = 6.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	11	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	11	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die. / Modified MOSFET symbol showing the internal device inductances. 
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

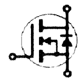
THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

UNITRODE CORPORATION • 5 FORBES ROAD
LEXINGTON, MA 02173 • TEL. (617) 861-6540
TWX (710) 326-6509 • TELEX 95-1064

PRINTED IN U.S.A.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN430 UFN431	–	–	4.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFN432 UFN433	–	–	4.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN430 UFN431	–	–	18	A	
		UFN432 UFN433	–	–	16	A	
V_{SD}	Diode Forward Voltage ②	UFN430 UFN431	–	–	1.4	V	$T_C = 25°C, I_S = 4.5A, V_{GS} = 0V$
		UFN432 UFN433	–	–	1.3	V	$T_C = 25°C, I_S = 4.0A, V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	–	800	–	ns	$T_J = 150°C, I_F = 4.5A, dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	–	4.6	–	μC	$T_J = 150°C, I_F = 4.5A, dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25°C$ to $150°C$. ② Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

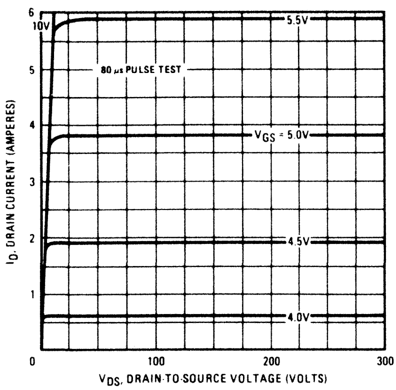


Fig. 2 — Typical Transfer Characteristics

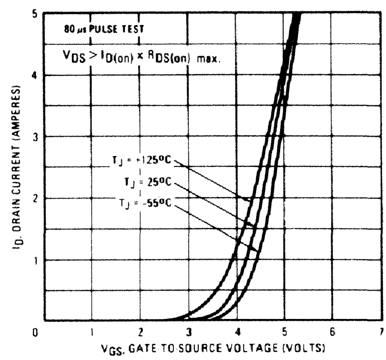


Fig. 3 — Typical Saturation Characteristics

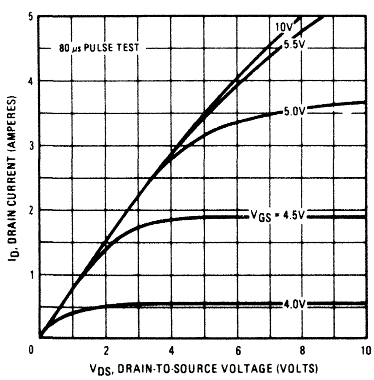


Fig. 4 — Maximum Safe Operating Area

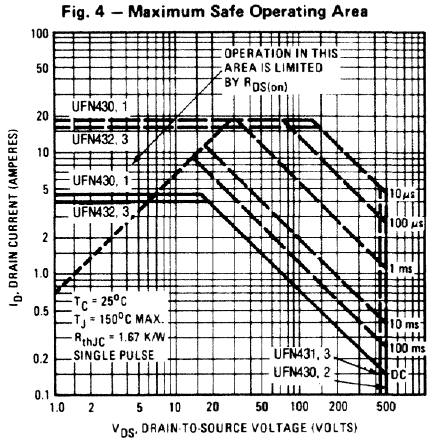


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

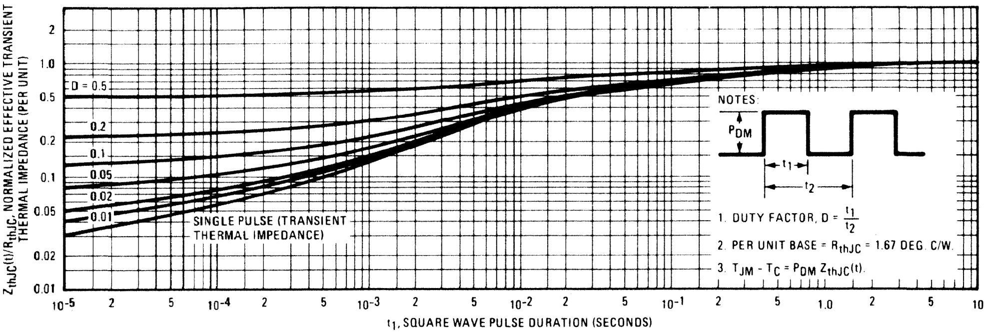


Fig. 6 — Typical Transconductance Vs. Drain Current

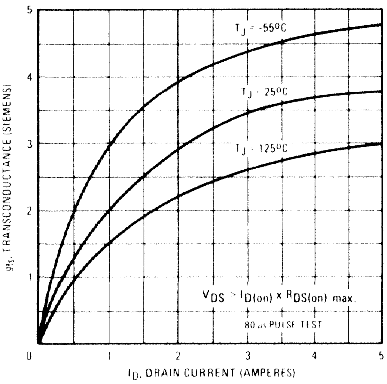


Fig. 7 — Typical Source-Drain Diode Forward Voltage

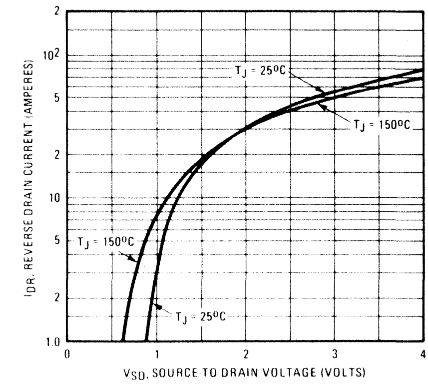


Fig. 8 — Breakdown Voltage Vs. Temperature

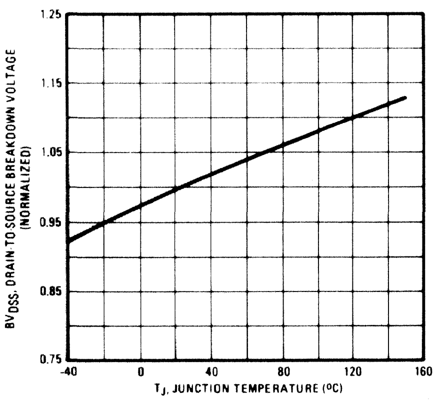


Fig. 9 — Normalized On-Resistance Vs. Temperature

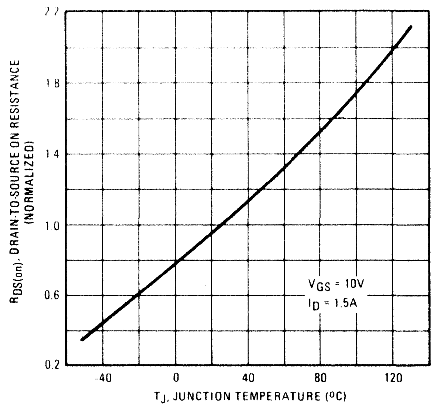


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

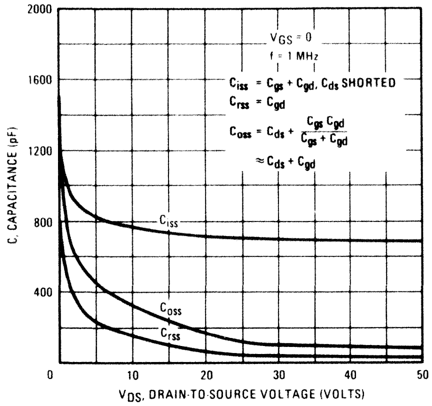


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

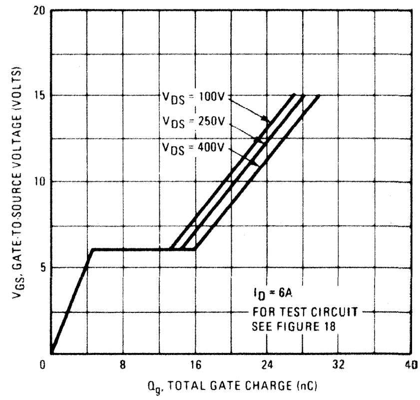


Fig. 12 — Typical On-Resistance Vs. Drain Current

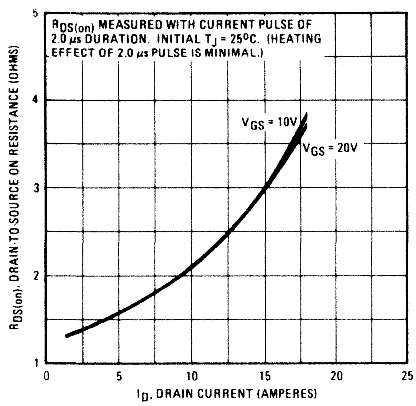


Fig. 13 — Maximum Drain Current Vs. Case Temperature

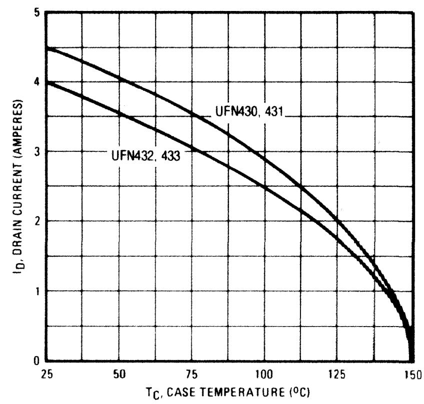


Fig. 14 — Power Vs. Temperature Derating Curve

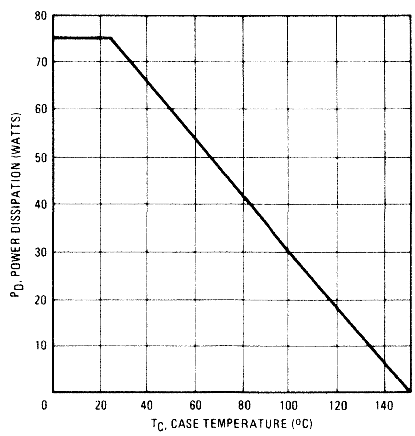


Fig. 15 — Clamped Inductive Test Circuit

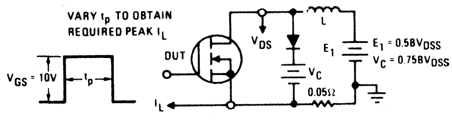


Fig. 16 — Clamped Inductive Waveforms

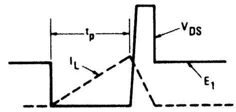


Fig. 17 — Switching Time Test Circuit

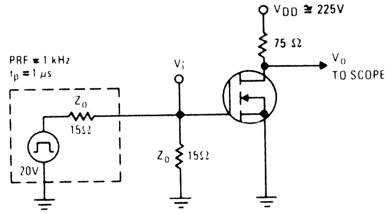
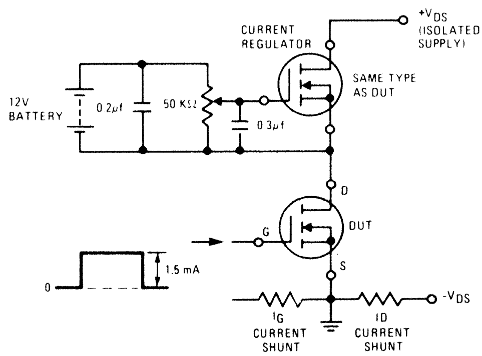


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

500 Volt, 0.85 Ohm
N-Channel

UFN440
UFN441
UFN442
UFN443

FEATURES
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

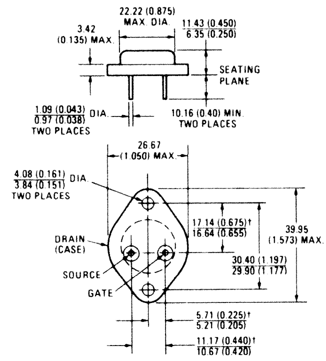
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN440	500V	0.85Ω	8.0A
UFN441	450V	0.85Ω	8.0A
UFN442	500V	1.10Ω	7.0A
UFN443	450V	1.10Ω	7.0A

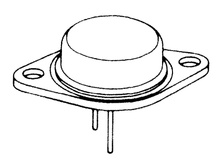
MECHANICAL SPECIFICATIONS

UFN440 UFN441 UFN442 UFN443



Dimensions in Millimeters and (Inches)

TO-3



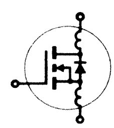
UNITRODE

ABSOLUTE MAXIMUM RATINGS

	Parameter	UFN440	UFN441	UFN442	UFN443	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_D @ T_C = 100°C	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_{DM}	Pulsed Drain Current ③	32	32	28	28	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 32	32	28	28	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

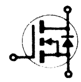
	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFN440 UFN442	500	—	—	V	V_{GS} = 0V
		UFN441 UFN443	450	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFN440 UFN441	8.0	—	—	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		UFN442 UFN443	7.0	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFN440 UFN441	—	0.8	0.85	Ω	V_{GS} = 10V, I_D = 4.0A
		UFN442 UFN443	—	1.0	1.1	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	6.5	—	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 4.0A
C_{iss}	Input Capacitance	ALL	—	1225	1600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	200	350	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	85	150	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	17	35	ns	V_{DD} ≈ 200V, I_D = 4.0A, Z_O = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	5	15	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	42	90	ns	
t_f	Fall Time	ALL	—	14	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	42	60	nC	V_{GS} = 10V, I_D = 10A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	20	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	22	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die. — Modified MOSFET symbol showing the internal device inductances.
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.



THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	—	—	1.0	K/W	
R_{thCS}	Case-to-Sink	ALL	—	0.1	—	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to Ambient	ALL	—	—	30	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN440 UFN441	—	—	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFN442 UFN443	—	—	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN440 UFN441	—	—	32	A	
		UFN442 UFN443	—	—	28	A	
V_{SD}	Diode Forward Voltage ②	UFN440 UFN441	—	—	2.0	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
		UFN442 UFN443	—	—	1.9	V	T_C = 25°C, I_S = 7.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	1100	—	ns	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	6.4	—	μC	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

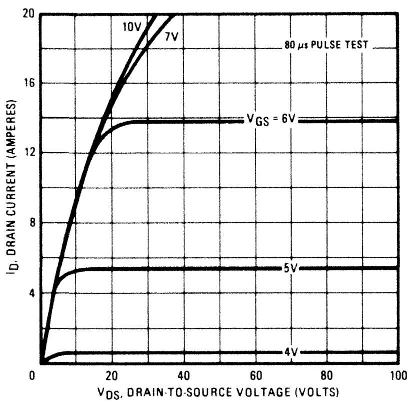


Fig. 2 — Typical Transfer Characteristics

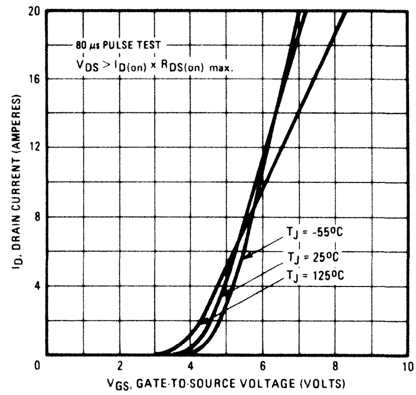


Fig. 3 — Typical Saturation Characteristics

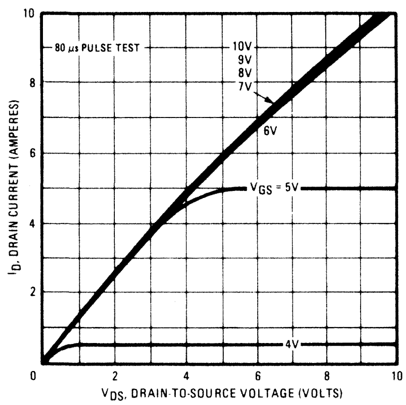


Fig. 4 — Maximum Safe Operating Area

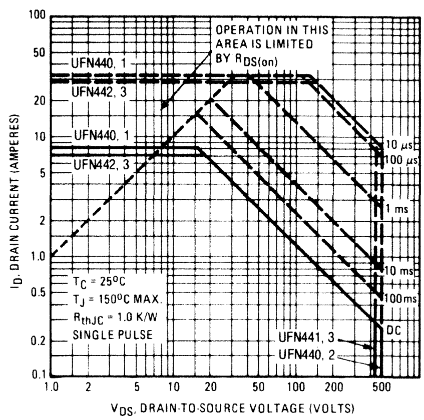


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

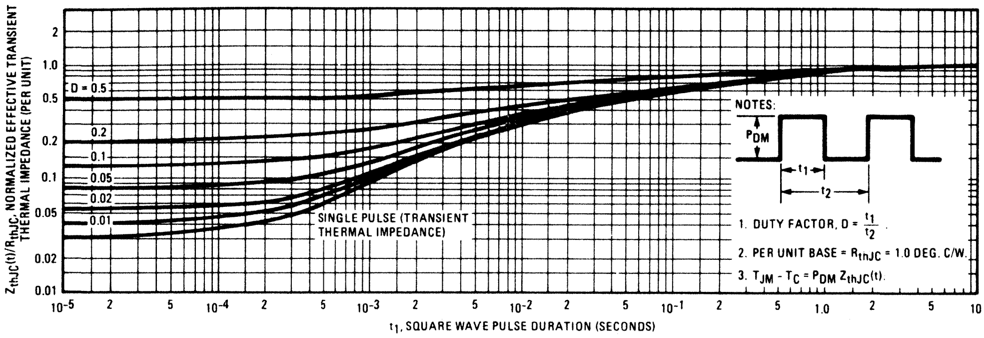


Fig. 6 — Typical Transconductance Vs. Drain Current

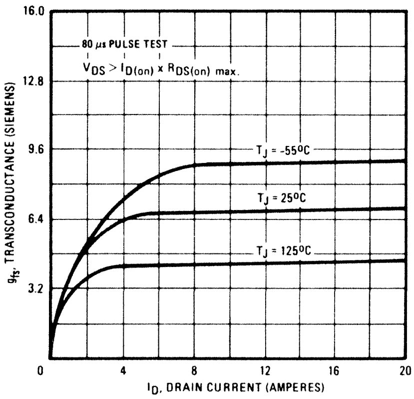


Fig. 7 — Typical Source-Drain Diode Forward Voltage

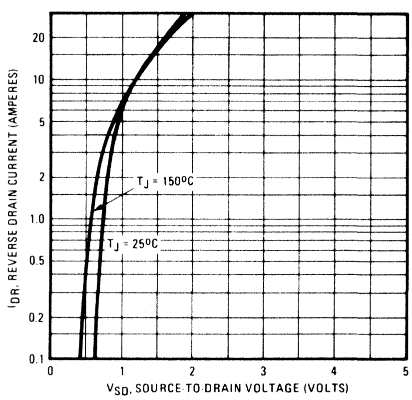


Fig. 8 — Breakdown Voltage Vs. Temperature

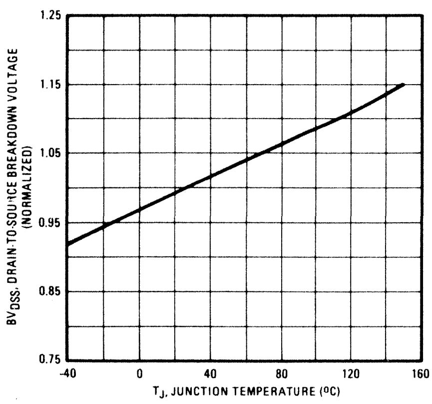


Fig. 9 — Normalized On-Resistance Vs. Temperature

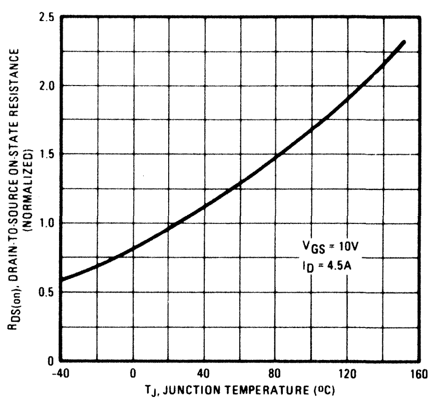


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

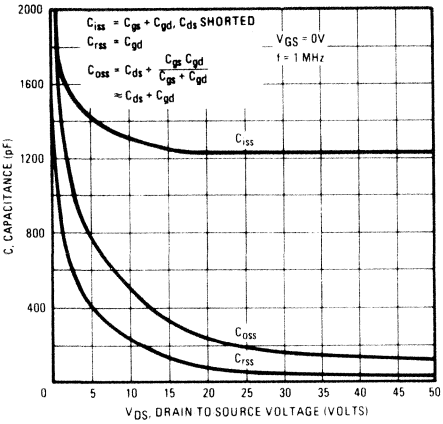


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

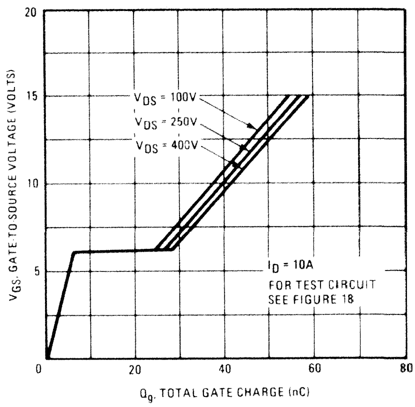


Fig. 12 – Typical On-Resistance Vs. Drain Current

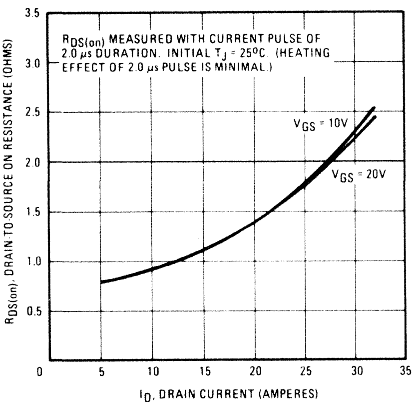


Fig. 13 – Maximum Drain Current Vs. Case Temperature

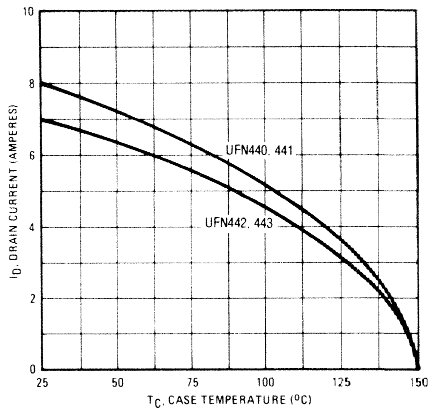


Fig. 14 – Power Vs. Temperature Derating Curve

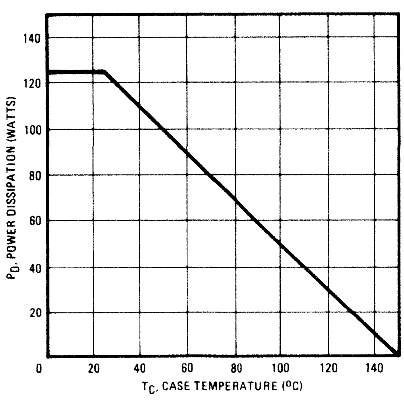


Fig. 15 — Clamped Inductive Test Circuit

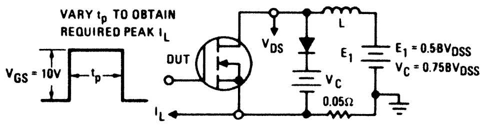


Fig. 16 — Clamped Inductive Waveforms

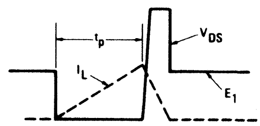


Fig. 17 — Switching Time Test Circuit

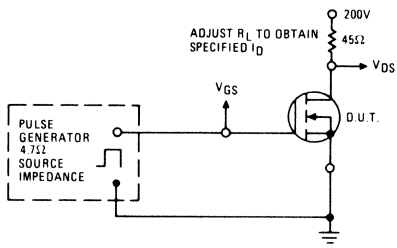
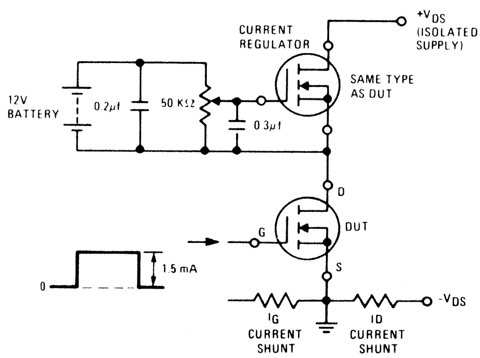


Fig. 18 — Gate Charge Test Circuit



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POWER MOSFET TRANSISTORS

500 Volt, 0.4 Ohm
N-Channel

UFN450
UFN451
UFN452
UFN453

FEATURES

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

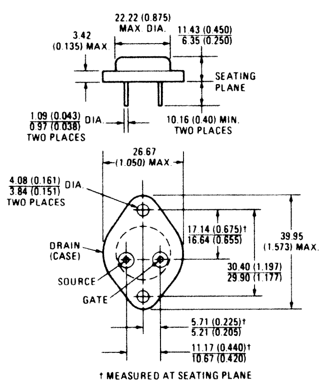
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN450	500V	0.4Ω	13A
UFN451	450V	0.4Ω	13A
UFN452	500V	0.5Ω	12A
UFN453	450V	0.5Ω	12A

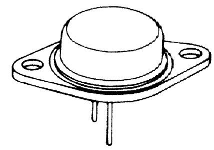
MECHANICAL SPECIFICATIONS

UFN450 UFN451 UFN452 UFN453



Dimensions in Millimeters and (Inches)

TO-3

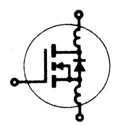


UNITRODE

ABSOLUTE MAXIMUM RATINGS

	Parameter	UFN450	UFN451	UFN452	UFN453	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	13	13	12	12	A
I_D @ T_C = 100°C	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_{DM}	Pulsed Drain Current ③	52	52	48	48	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	150 (See Fig. 14)				W
	Linear Derating Factor	1.2 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 14 and 15) L = 100μH 52	52	48	48	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

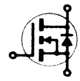
ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFN450 UFN452	500	—	—	V	V_{GS} = 0V
		UFN451 UFN453	450	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFN450 UFN451	13	—	—	A	V_{DS} › $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		UFN452 UFN453	12	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFN450 UFN451	—	0.3	0.4	Ω	V_{GS} = 10V, I_D = 7.0A
		UFN452 UFN453	—	0.4	0.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	6.0	11	—	S (℧)	V_{DS} › $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 7.0A
C_{iss}	Input Capacitance	ALL	—	2000	3000	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	400	600	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	100	200	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	—	35	ns	V_{DD} ≈ 210V, I_D = 7.0A, Z_O = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	—	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	—	150	ns	
t_f	Fall Time	ALL	—	—	70	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	82	120	nC	V_{GS} = 10V, I_D = 16A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	40	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	42	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die. — Modified MOSFET symbol showing the internal device inductances. 
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	—	—	.83	K/W	
R_{thCS}	Case-to Sink	ALL	—	0.1	—	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN450 UFN451	—	—	13	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFN452 UFN453	—	—	12	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN450 UFN451	—	—	52	A	
		UFN452 UFN453	—	—	48	A	
V_{SD}	Diode Forward Voltage ②	UFN450 UFN451	—	—	1.4	V	$T_C = 25°C, I_S = 13A, V_{GS} = 0V$
		UFN452 UFN453	—	—	1.3	V	$T_C = 25°C, I_S = 12A, V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	1300	—	ns	$T_J = 150°C, I_F = 13A, dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	7.4	—	μC	$T_J = 150°C, I_F = 13A, dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25°C$ to $150°C$. ② Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

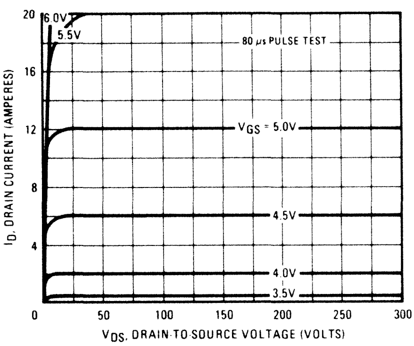


Fig. 2 — Typical Transfer Characteristics

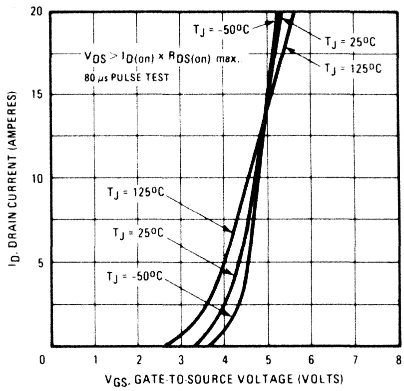


Fig. 3 — Typical Saturation Characteristics

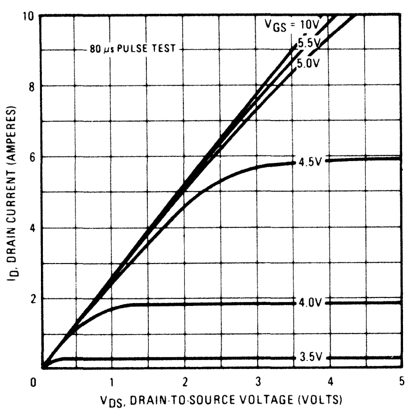


Fig. 4 — Maximum Safe Operating Area

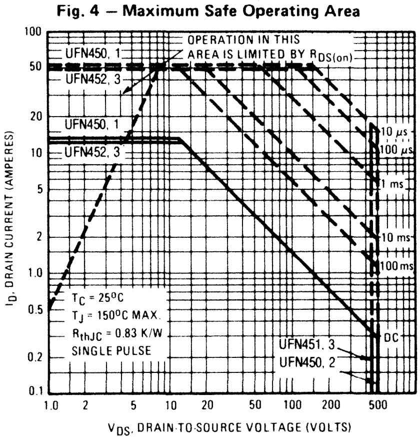


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

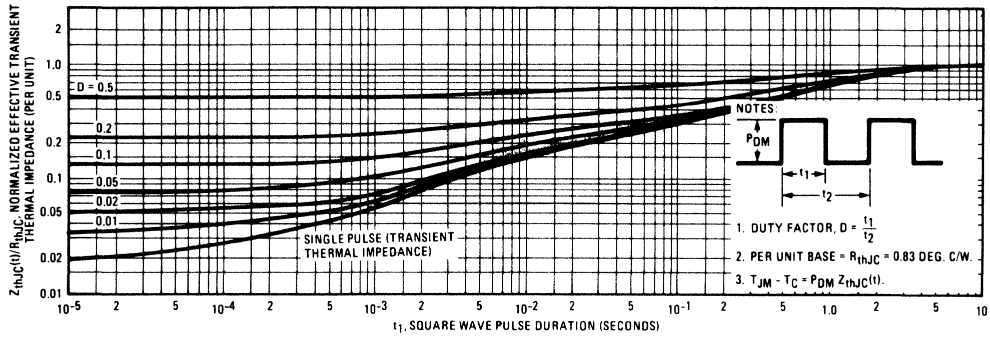


Fig. 6 — Typical Transconductance Vs. Drain Current

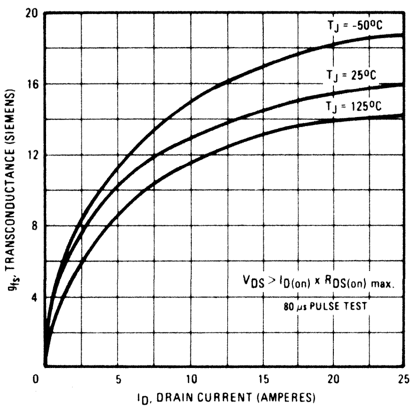


Fig. 7 — Typical Source-Drain Diode Forward Voltage

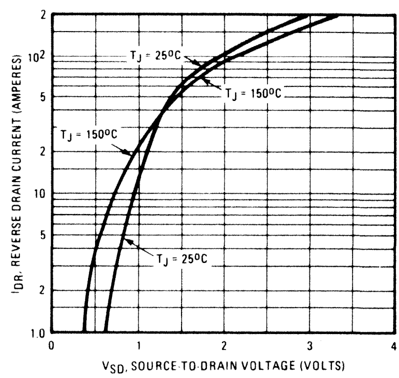


Fig. 8 — Breakdown Voltage Vs. Temperature

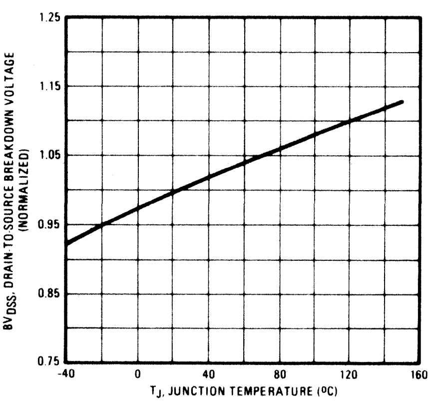


Fig. 9 — Normalized On-Resistance Vs. Temperature

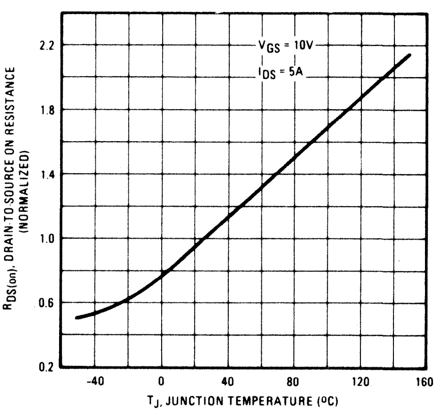


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

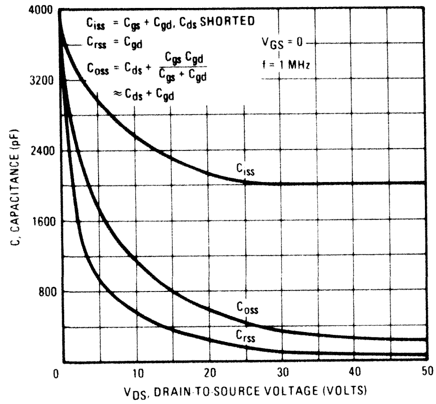


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

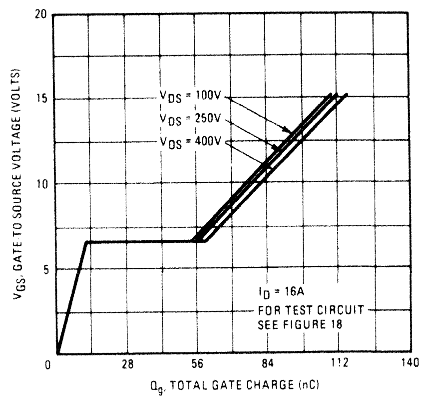


Fig. 12 — Typical On-Resistance Vs. Drain Current

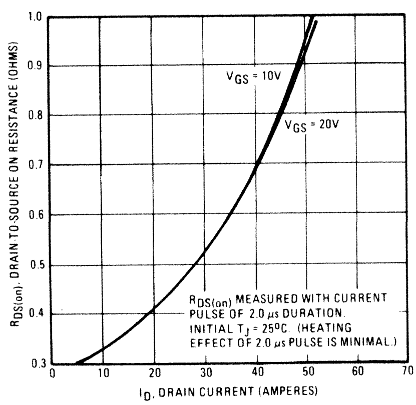


Fig. 13 — Maximum Drain Current Vs. Case Temperature

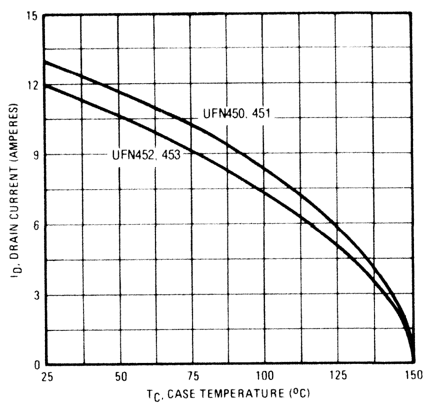


Fig. 14 — Power Vs. Temperature Derating Curve

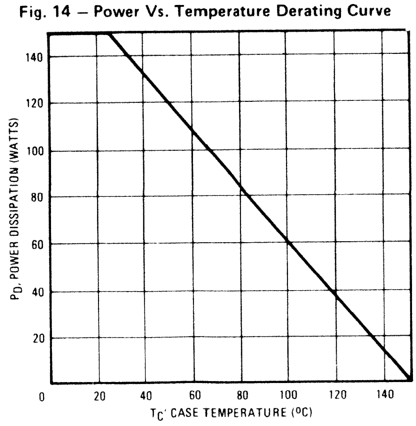


Fig. 15 — Clamped Inductive Test Circuit

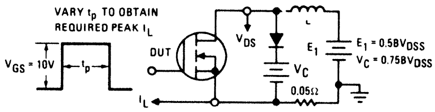


Fig. 16 — Clamped Inductive Waveforms

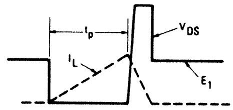


Fig. 17 — Switching Time Test Circuit

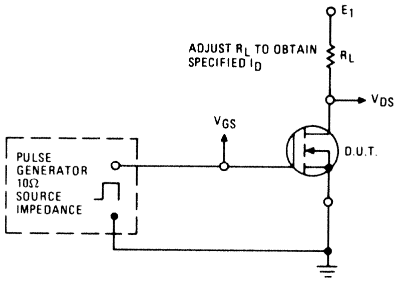
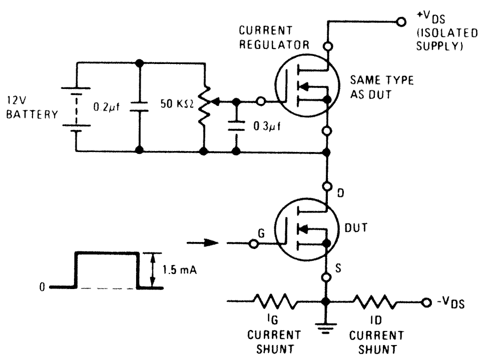


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

100 Volt, 0.6 Ohm
N-Channel

UFN510
UFN511
UFN512
UFN513

FEATURES

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

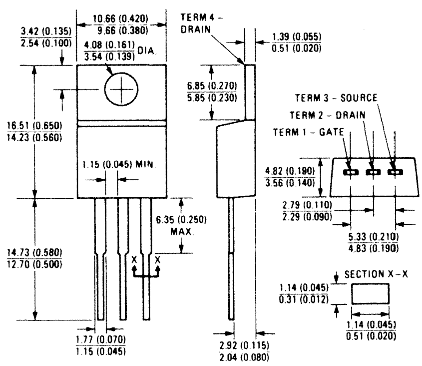
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN510	100V	0.6Ω	4.0A
UFN511	60V	0.6Ω	4.0A
UFN512	100V	0.8Ω	3.5A
UFN513	60V	0.8Ω	3.5A

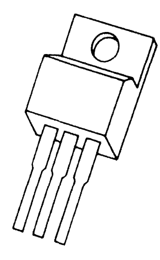
MECHANICAL SPECIFICATIONS

UFN510 UFN511 UFN512 UFN513



Dimensions in Millimeters and (Inches)

TO-220AB



4/83

UNITRODE

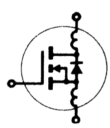
ABSOLUTE MAXIMUM RATINGS

Parameter		UFN510	UFN511	UFN512	UFN513	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	4.0	4.0	3.5	3.5	A
I_D @ T_C = 100°C	Continuous Drain Current	2.5	2.5	2.0	2.0	A
I_{DM}	Pulsed Drain Current ③	16	16	14	14	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 16	16	14	14	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFN510 UFN512	100	—	—	V	V_{GS} = 0V
		UFN511 UFN513	60	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFN510 UFN511	4.0	—		A	$V_{DS} > I_{D(on)} \times R_{DS(on)\,max.}$, V_{GS} = 10V
		UFN512 UFN513	3.5	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFN510 UFN511	—	0.5	0.6	Ω	V_{GS} = 10V, I_D = 2.0A
		UFN512 UFN513		0.6	0.8	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	1.5	—	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)\,max.}$, I_D = 2.0A
C_{iss}	Input Capacitance	ALL	—	135	150	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	80	100	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	20	25	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	10	20	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 2.0A, Z_O = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	15	25	ns	
t_f	Fall Time	ALL	—	10	20	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	5.0	7.5	nC	V_{GS} = 10V, I_D = 8.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	2.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	3.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.
			—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

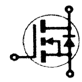
Modified MOSFET symbol showing the internal device inductances.



THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	—	—	6.4	K/W	
R_{thCS}	Case-to-Sink	ALL	—	1.0	—	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN510 UFN511	—	—	4.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFN512 UFN513	—	—	3.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN510 UFN511	—	—	16	A	
		UFN512 UFN513	—	—	14	A	
V_{SD}	Diode Forward Voltage ②	UFN510 UFN511	—	—	2.5	V	T_C = 25°C, I_S = 4.0A, V_{GS} = 0V
		UFN512 UFN513	—	—	2.0	V	T_C = 25°C, I_S = 3.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	230	—	ns	T_J = 150°C, I_F = 4.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	1.4	—	μC	T_J = 150°C, I_F = 4.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

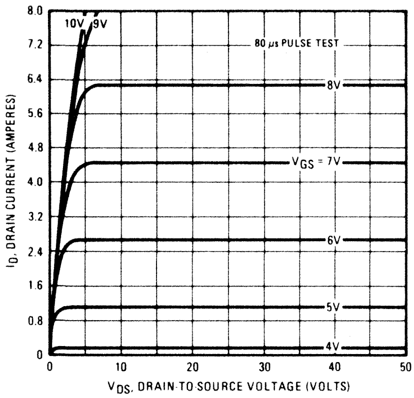


Fig. 2 — Typical Transfer Characteristics

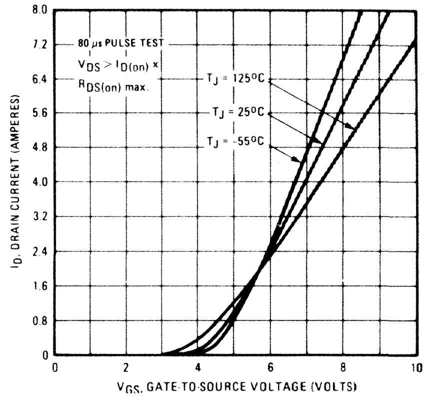


Fig. 3 — Typical Saturation Characteristics

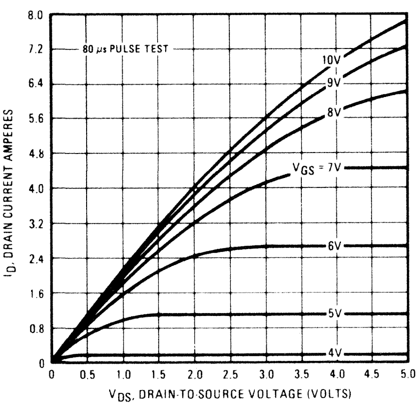


Fig. 4 — Maximum Safe Operating Area

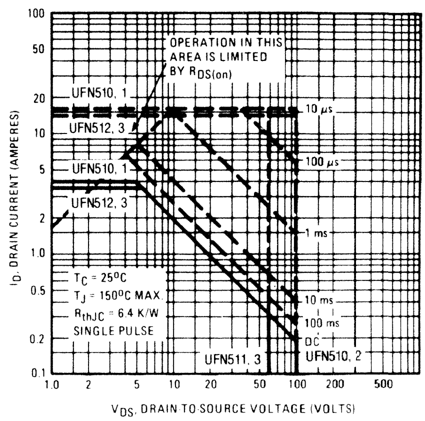


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

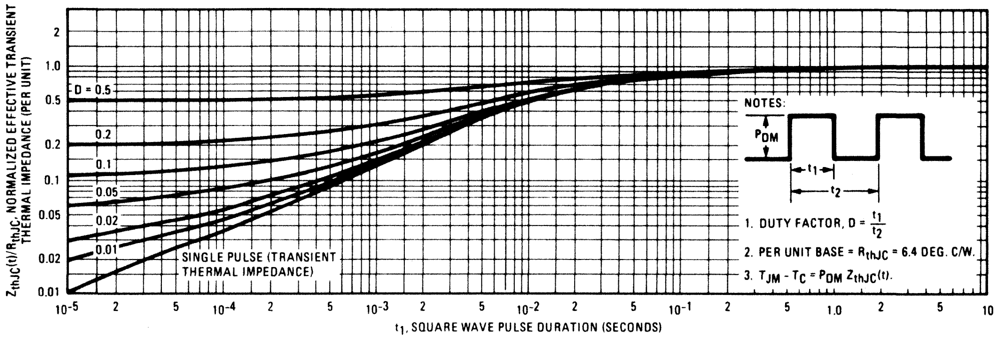


Fig. 6 — Typical Transconductance Vs. Drain Current

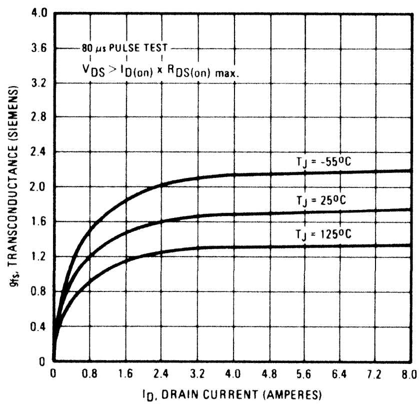


Fig. 7 — Typical Source-Drain Diode Forward Voltage

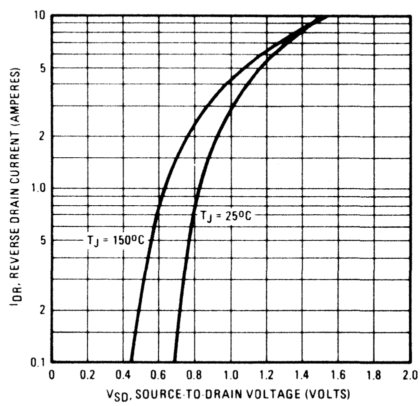


Fig. 8 — Breakdown Voltage Vs. Temperature

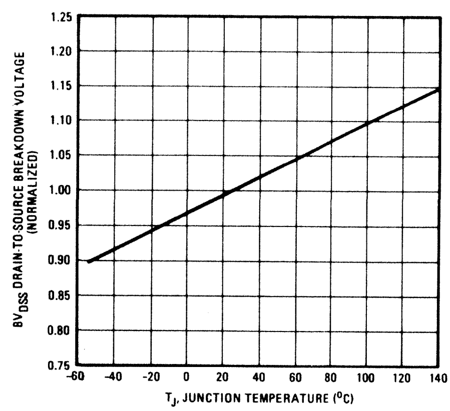


Fig. 9 — Normalized On-Resistance Vs. Temperature

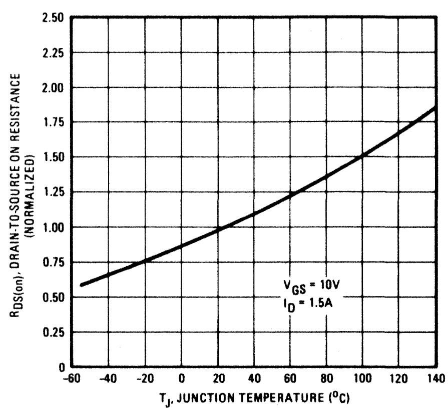


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

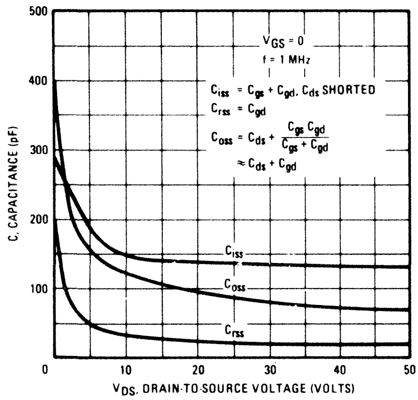


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

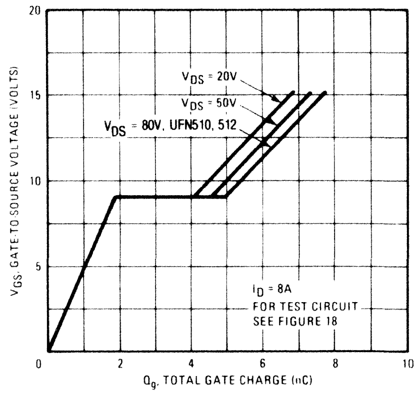


Fig. 12 – Typical On-Resistance Vs. Drain Current

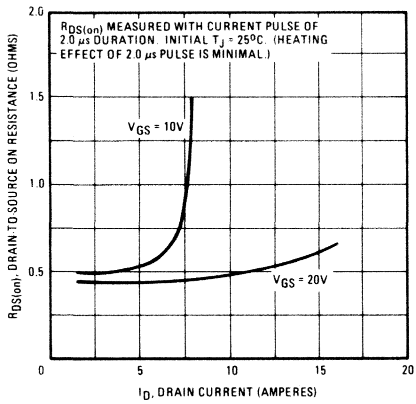


Fig. 13 – Maximum Drain Current Vs. Case Temperature

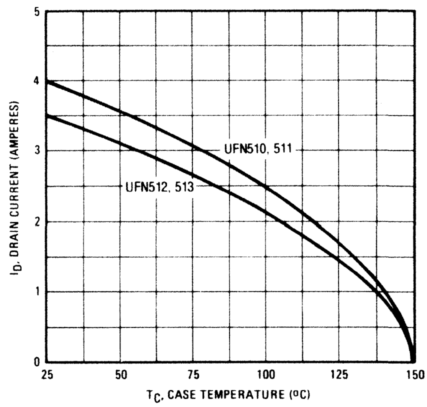


Fig. 14 – Power Vs. Temperature Derating Curve

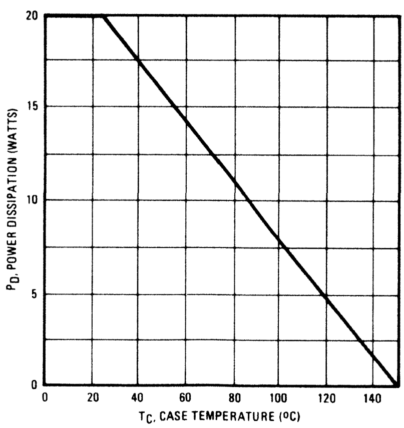


Fig. 15 — Clamped Inductive Test Circuit

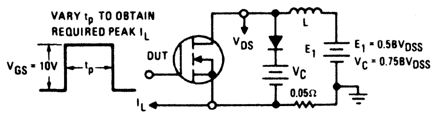


Fig. 16 — Clamped Inductive Waveforms

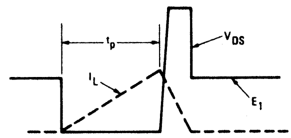


Fig. 17 — Switching Time Test Circuit

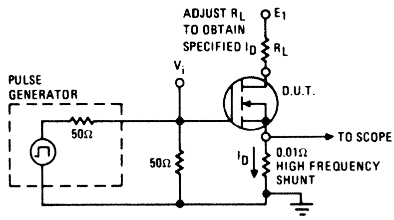
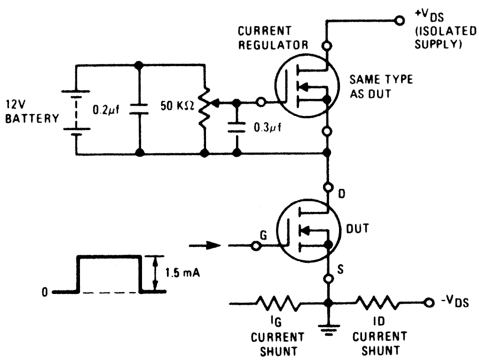


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

100 Volt, 0.3 Ohm
N-Channel

UFN520
UFN521
UFN522
UFN523

FEATURES

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

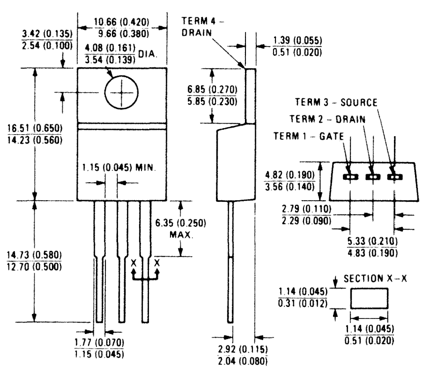
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN520	100V	0.30Ω	8.0A
UFN521	60V	0.30Ω	8.0A
UFN522	100V	0.40Ω	7.0A
UFN523	60V	0.40Ω	7.0A

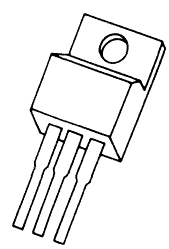
MECHANICAL SPECIFICATIONS

UFN520 UFN521 UFN522 UFN523



Dimensions in Millimeters and (Inches)

TO-220AB

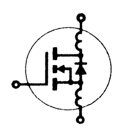


UNITRODE

ABSOLUTE MAXIMUM RATINGS

Parameter		UFN520	UFN521	UFN522	UFN523	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_D @ T_C = 100°C	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_{DM}	Pulsed Drain Current ③	32	32	28	28	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 32	32	28	28	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

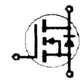
ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFN520 UFN522	100	–	–	V	V_{GS} = 0V
		UFN521 UFN523	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFN520 UFN521	8.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		UFN522 UFN523	7.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFN520 UFN521	–	0.25	0.30	Ω	V_{GS} = 10V, I_D = 4.0A
		UFN522 UFN523	–	0.30	0.40	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.5	2.9	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 4.0A
C_{iss}	Input Capacitance	ALL	–	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	200	400	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	50	100	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 4.0A, Z_O = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	35	70	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	35	70	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	10	15	nC	V_{GS} = 15V, I_D = 10A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	6.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	4.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die. / Modified MOSFET symbol showing the internal device inductances.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad. 

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	K/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN520 UFN521	—	—	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFN522 UFN523	—	—	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN520 UFN521	—	—	32	A	
		UFN522 UFN523	—	—	28	A	
V_{SD}	Diode Forward Voltage ②	UFN520 UFN521	—	—	2.5	V	$T_C = 25°C, I_S = 8.0A, V_{GS} = 0V$
		UFN522 UFN523	—	—	2.3	V	$T_C = 25°C, I_S = 7.0A, V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	280	—	ns	$T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	1.6	—	μC	$T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

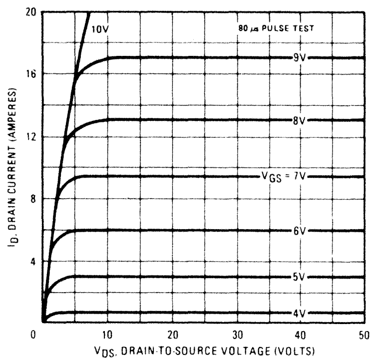


Fig. 2 — Typical Transfer Characteristics

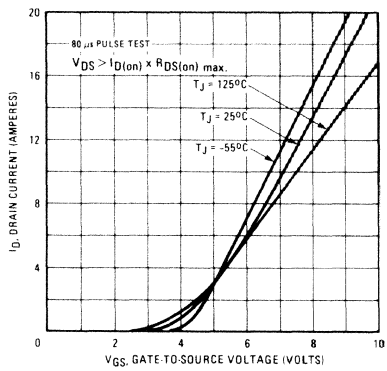


Fig. 3 — Typical Saturation Characteristics

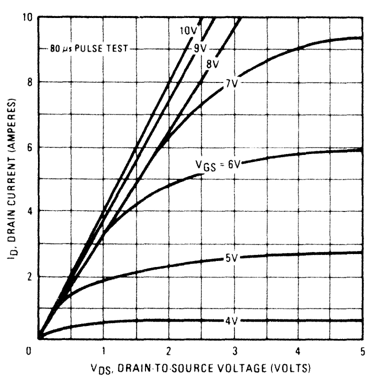


Fig. 4 — Maximum Safe Operating Area

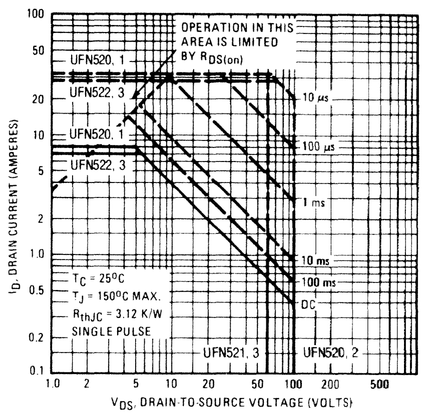


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

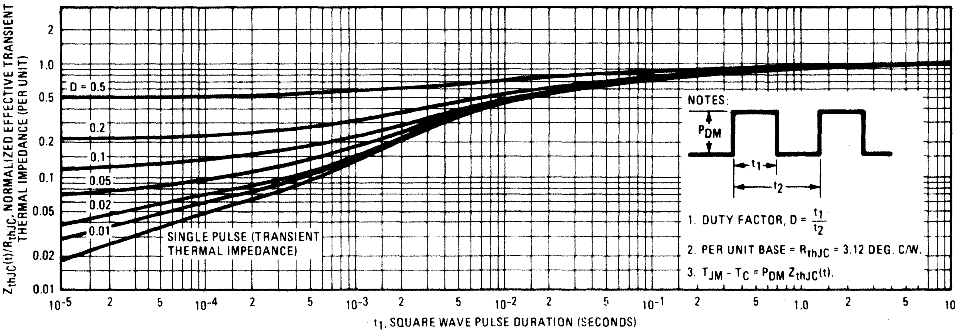


Fig. 6 — Typical Transconductance Vs. Drain Current

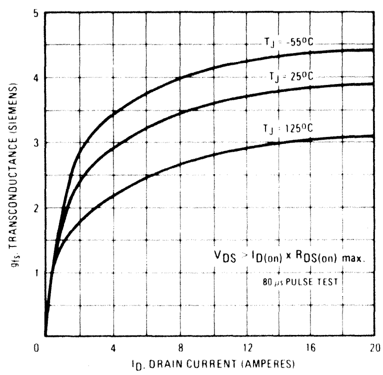


Fig. 7 — Typical Source-Drain Diode Forward Voltage

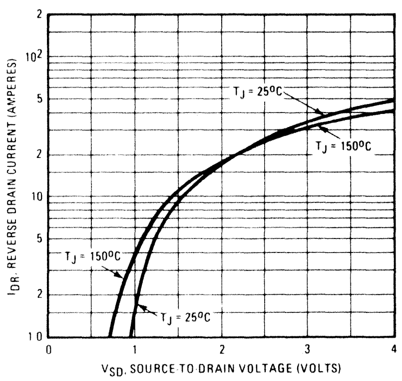


Fig. 8 — Breakdown Voltage Vs. Temperature

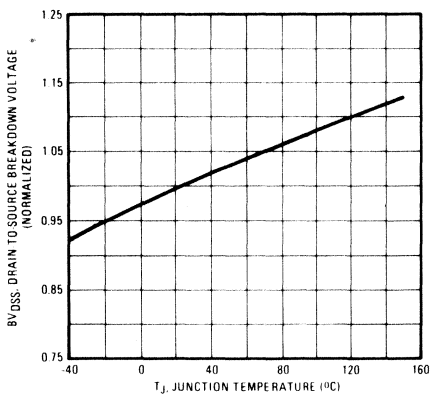


Fig. 9 — Normalized On-Resistance Vs. Temperature

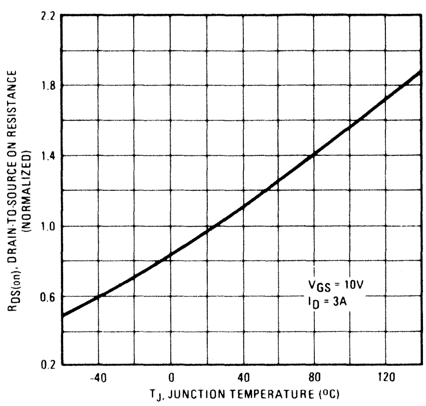


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Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

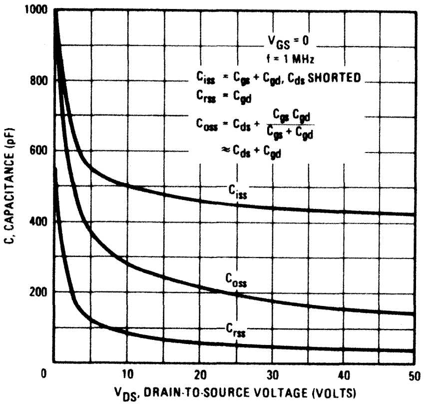


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

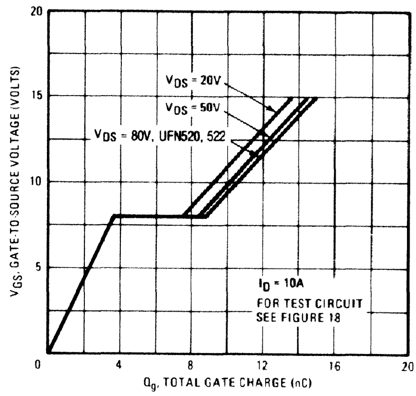


Fig. 12 — Typical On-Resistance Vs. Drain Current

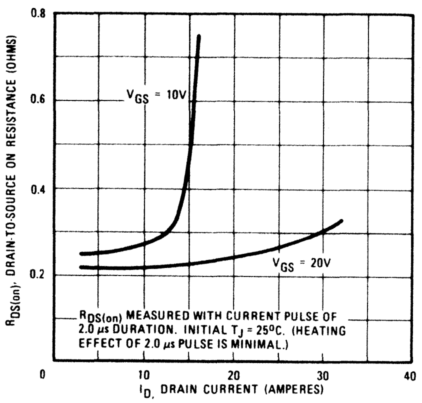


Fig. 13 — Maximum Drain Current Vs. Case Temperature

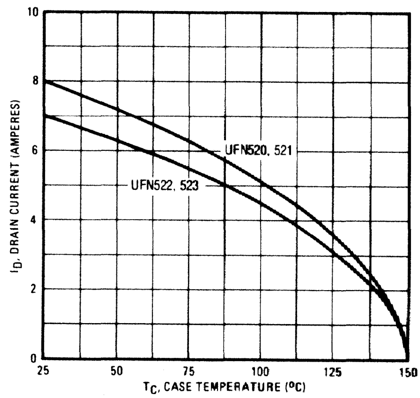


Fig. 14 — Power Vs. Temperature Derating Curve

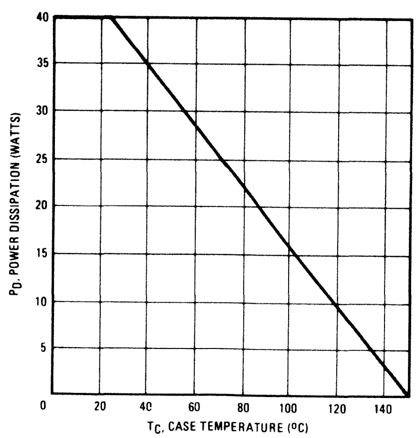


Fig. 15 — Clamped Inductive Test Circuit

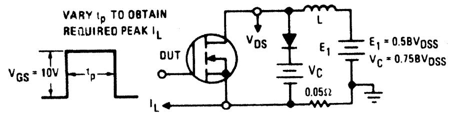


Fig. 16 — Clamped Inductive Waveforms

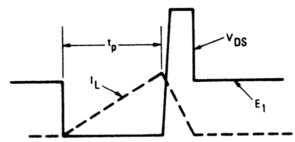


Fig. 17 — Switching Time Test Circuit

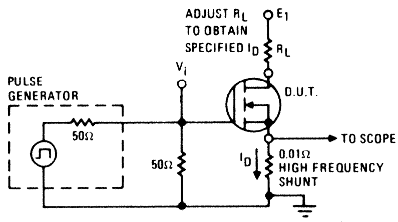
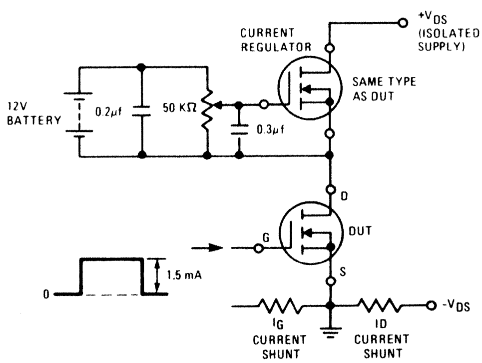


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

100 Volt, 0.18 Ohm
N-Channel

UFN530
UFN531
UFN532
UFN533

FEATURES
- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

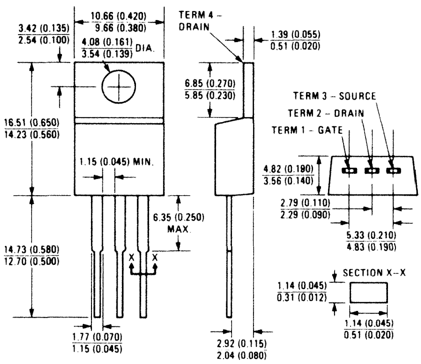
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN530	100V	0.18Ω	14A
UFN531	60V	0.18Ω	14A
UFN532	100V	0.25Ω	12A
UFN533	60V	0.25Ω	12A

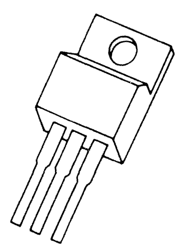
MECHANICAL SPECIFICATIONS

UFN530 UFN531 UFN532 UFN533



Dimensions in Millimeters and (Inches)

TO-220AB

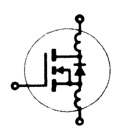


UNITRODE

ABSOLUTE MAXIMUM RATINGS

Parameter		UFN530	UFN531	UFN532	UFN533	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	14	14	12	12	A
I_D @ T_C = 100°C	Continuous Drain Current	9.0	9.0	8.0	8.0	A
I_{DM}	Pulsed Drain Current ③	56	56	48	48	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 56	56	48	48	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

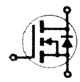
ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFN530 UFN532	100	—	—	V	V_{GS} = 0V
		UFN531 UFN533	60	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFN530 UFN531	14	—	—	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		UFN532 UFN533	12	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFN530 UFN531	—	0.14	0.18	Ω	V_{GS} = 10V, I_D = 8.0A
		UFN532 UFN533	—	0.20	0.25	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	5.5	—	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 8.0A
C_{iss}	Input Capacitance	ALL	—	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	300	500	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	100	150	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	—	30	ns	V_{DD} = 36V, I_D = 8.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	—	75	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	—	40	ns	
t_f	Fall Time	ALL	—	—	45	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	18	30	nC	V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	9.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	9.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die. — Modified MOSFET symbol showing the internal device inductances. 
			—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	—	—	1.67	K/W	
R_{thCS}	Case-to-Sink	ALL	—	1.0	—	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN530 UFN531	—	—	14	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFN532 UFN533	—	—	12	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN530 UFN531	—	—	56	A	
		UFN532 UFN533	—	—	48	A	
V_{SD}	Diode Forward Voltage ②	UFN530 UFN531	—	—	2.5	V	$T_C = 25°C$, $I_S = 14A$, $V_{GS} = 0V$
		UFN532 UFN533	—	—	2.3	V	$T_C = 25°C$, $I_S = 12A$, $V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	360	—	ns	$T_J = 150°C$, $I_F = 14A$, $dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	2.1	—	μC	$T_J = 150°C$, $I_F = 14A$, $dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25°C$ to $150°C$. ② Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

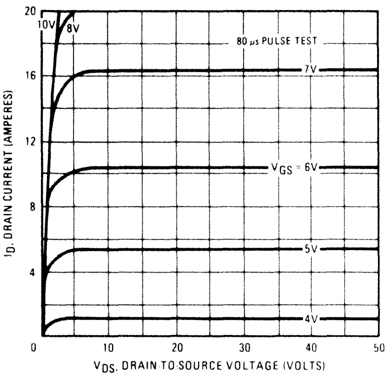


Fig. 2 — Typical Transfer Characteristics

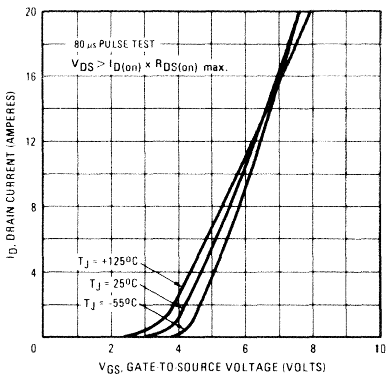


Fig. 3 — Typical Saturation Characteristics

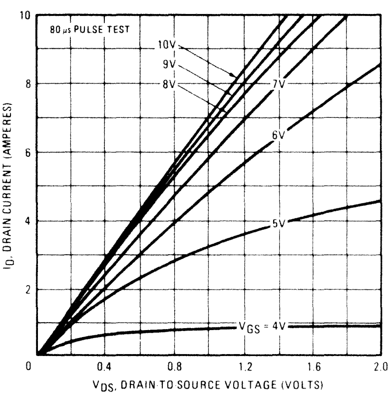


Fig. 4 — Maximum Safe Operating Area

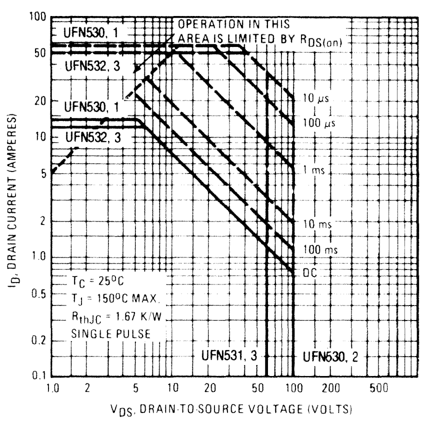


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

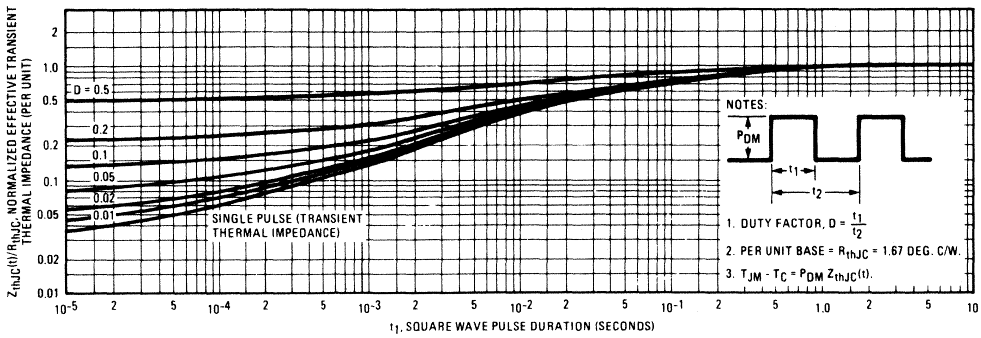


Fig. 6 — Typical Transconductance Vs. Drain Current

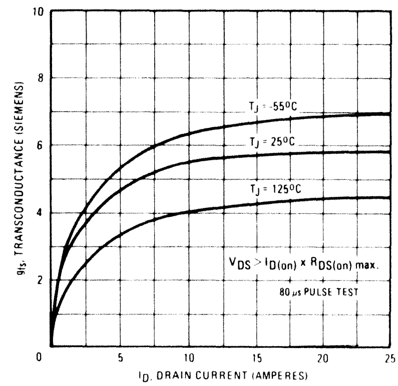


Fig. 7 — Typical Source-Drain Diode Forward Voltage

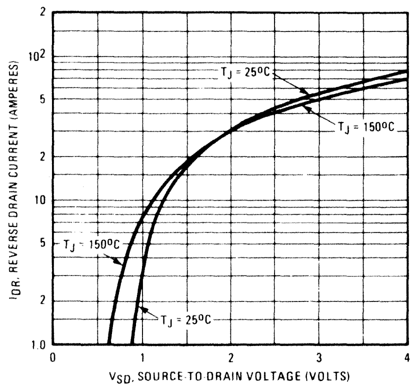


Fig. 8 — Breakdown Voltage Vs. Temperature

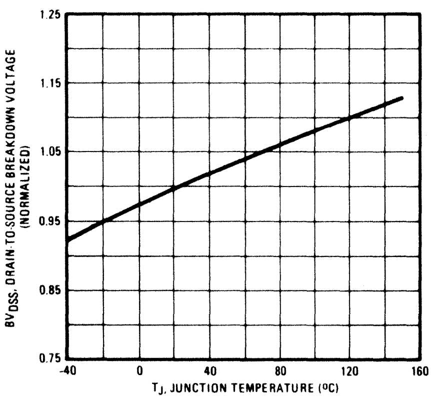


Fig. 9 — Normalized On-Resistance Vs. Temperature

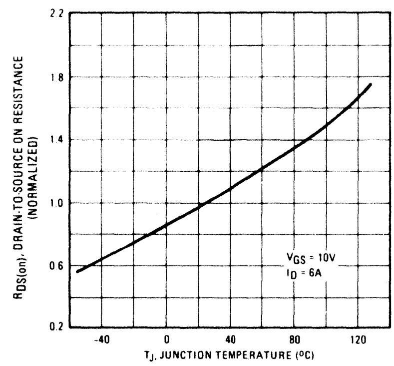


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

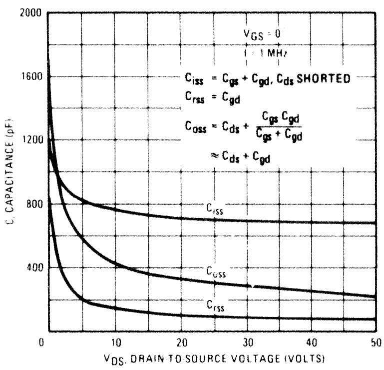


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

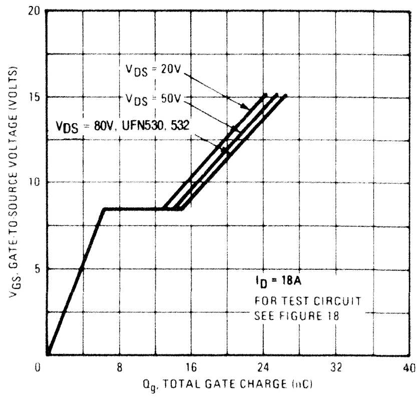


Fig. 12 – Typical On-Resistance Vs. Drain Current

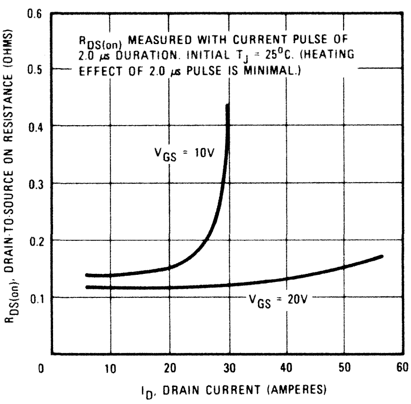


Fig. 13 – Maximum Drain Current Vs. Case Temperature

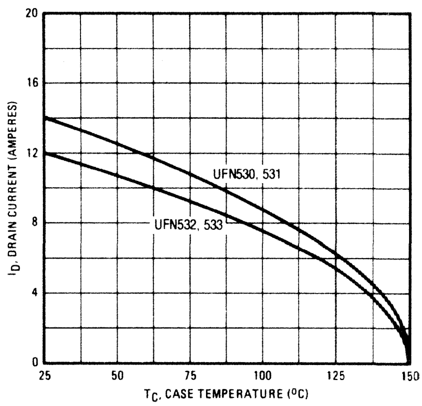


Fig. 14 – Power Vs. Temperature Derating Curve

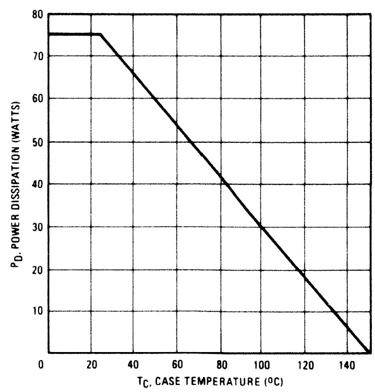


Fig. 15 — Clamped Inductive Test Circuit

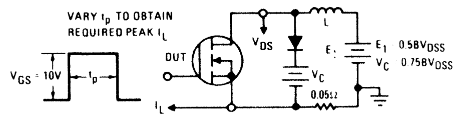


Fig. 16 — Clamped Inductive Waveforms

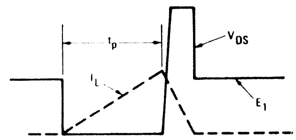


Fig. 17 — Switching Time Test Circuit

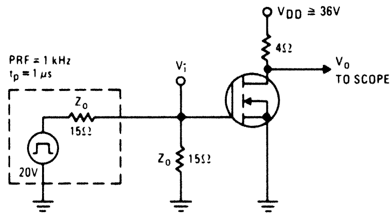
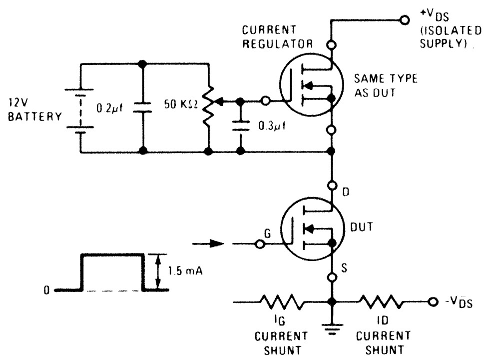


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

100 Volt, 0.085 Ohm
N-Channel

UFN540
UFN541
UFN542
UFN543

FEATURES

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

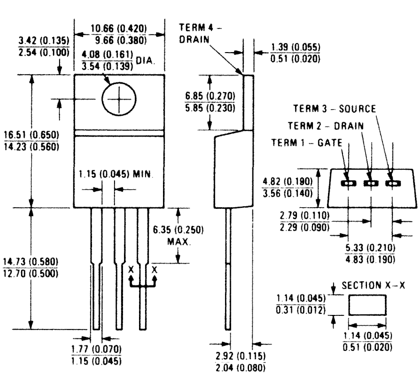
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN540	100V	0.085Ω	27A
UFN541	60V	0.085Ω	27A
UFN542	100V	0.11Ω	24A
UFN543	60V	0.11Ω	24A

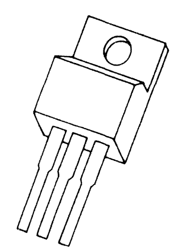
MECHANICAL SPECIFICATIONS

UFN540 UFN541 UFN542 UFN543



Dimensions in Millimeters and (Inches)

TO-220AB



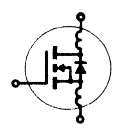
UNITRODE

ABSOLUTE MAXIMUM RATINGS

Parameter		UFN540	UFN541	UFN542	UFN543	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	27	27	24	24	A
I_D @ T_C = 100°C	Continuous Drain Current	17	17	15	15	A
I_{DM}	Pulsed Drain Current ③	108	108	96	96	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 108	108	96	96	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

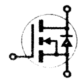
Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFN540 UFN542	100	–	–	V	V_{GS} = 0V
		UFN541 UFN543	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFN540 UFN541	27	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		UFN542 UFN543	24	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFN540 UFN541	–	0.07	0.085	Ω	V_{GS} = 10V, I_D = 15A
		UFN542 UFN543	–	0.09	0.11	Ω	
g_{fs}	Forward Transconductance ②	ALL	6.0	10	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 15A
C_{iss}	Input Capacitance	ALL	–	1275	1600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	550	800	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	160	300	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	16	30	ns	V_{DD} = 30V, I_D = 15A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	27	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	38	80	ns	
t_f	Fall Time	ALL	–	14	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	38	60	nC	V_{GS} = 10V, I_D = 34A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	17	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	21	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die. / Modified MOSFET symbol showing the internal device inductances.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.



THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	1.0	K/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN540 UFN541	—	—	27	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFN542 UFN543	—	—	24	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN540 UFN541	—	—	108	A	
		UFN542 UFN543	—	—	96	A	
V_{SD}	Diode Forward Voltage ②	UFN540 UFN541	—	—	2.5	V	$T_C = 25°C, I_S = 27A, V_{GS} = 0V$
		UFN542 UFN543	—	—	2.3	V	$T_C = 25°C, I_S = 24A, V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	500	—	ns	$T_J = 150°C, I_F = 27A, dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	2.9	—	μC	$T_J = 150°C, I_F = 27A, dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25°C$ to $150°C$. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

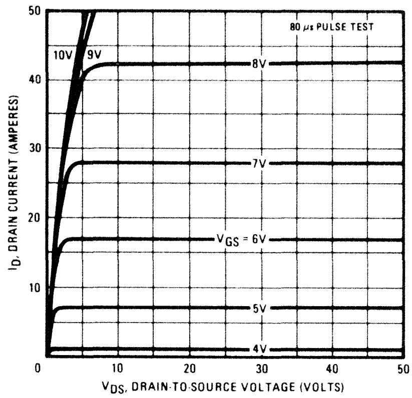


Fig. 2 — Typical Transfer Characteristics

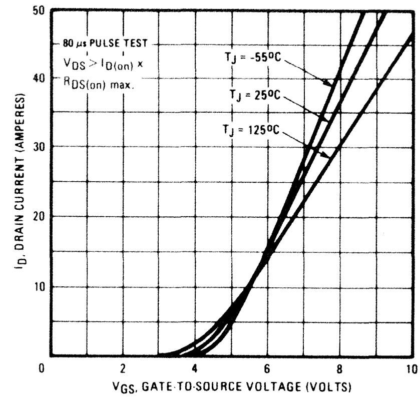


Fig. 3 — Typical Saturation Characteristics

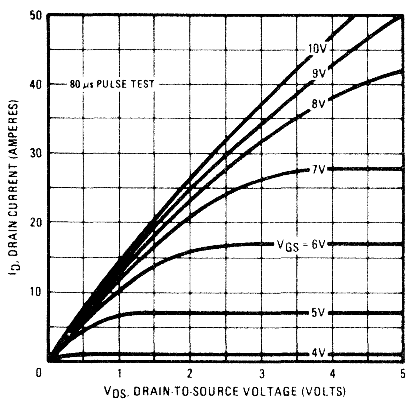


Fig. 4 — Maximum Safe Operating Area

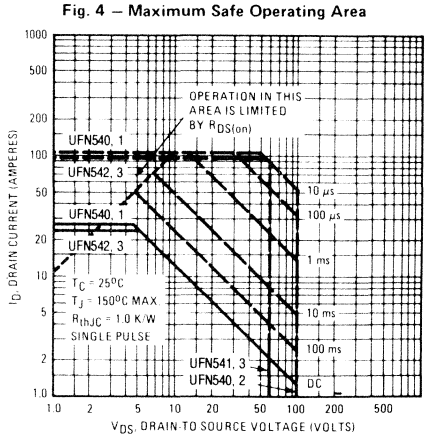


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

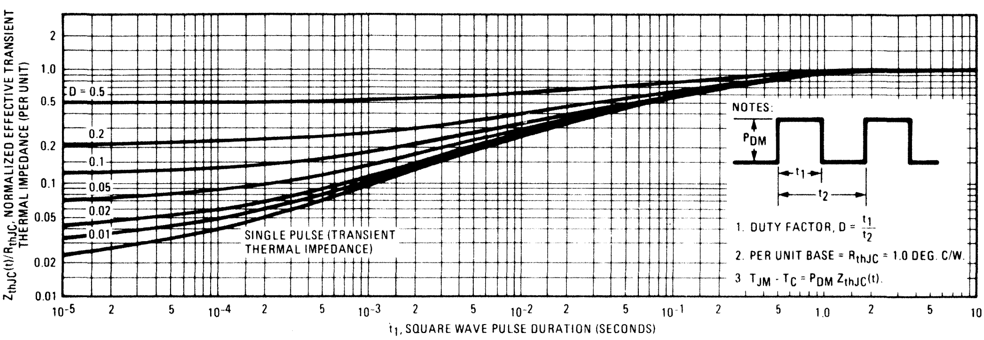


Fig. 6 — Typical Transconductance Vs. Drain Current

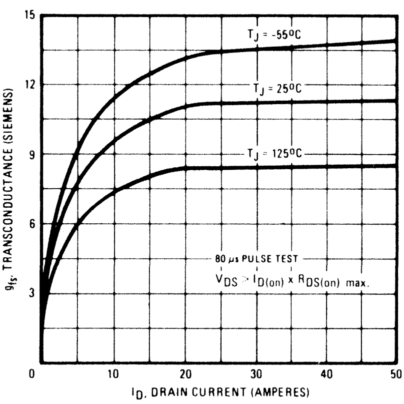


Fig. 7 — Typical Source-Drain Diode Forward Voltage

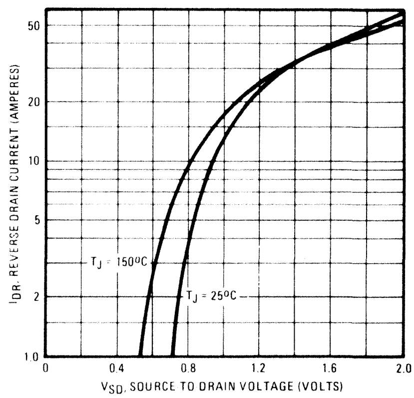


Fig. 8 — Breakdown Voltage Vs. Temperature

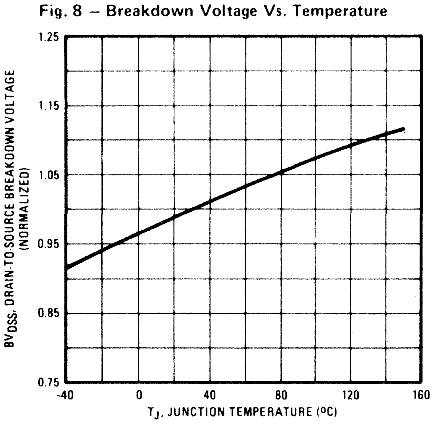


Fig. 9 — Normalized On-Resistance Vs. Temperature

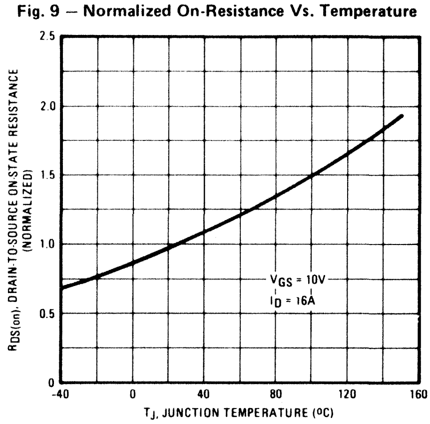


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

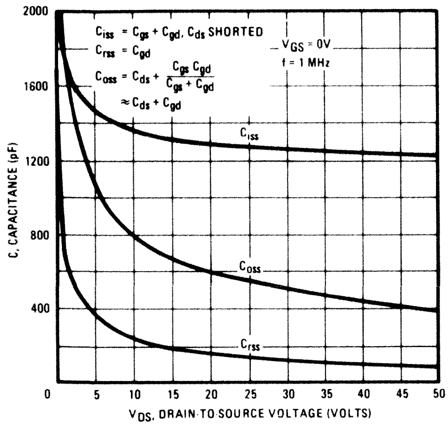


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

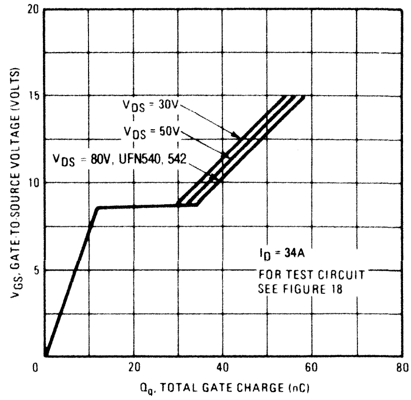


Fig. 12 – Typical On-Resistance Vs. Drain Current

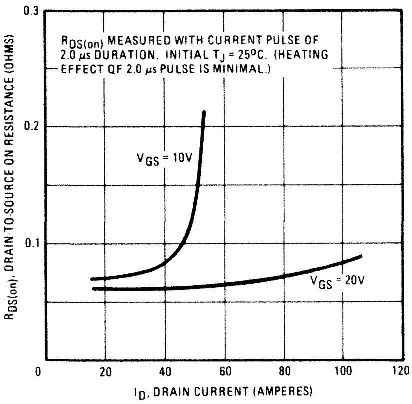


Fig. 13 – Maximum Drain Current Vs. Case Temperature

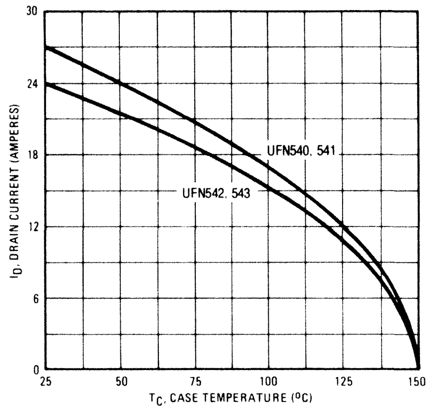


Fig. 14 – Power Vs. Temperature Derating Curve

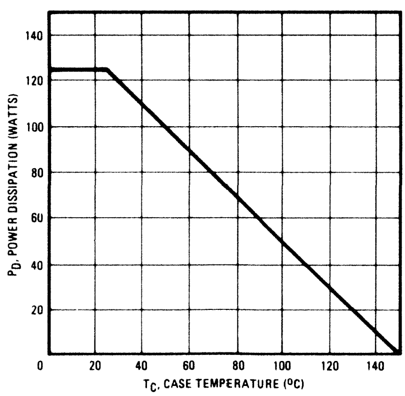


Fig. 15 – Clamped Inductive Test Circuit

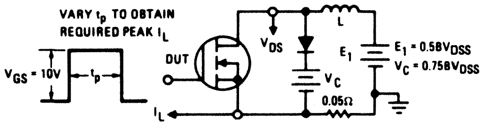


Fig. 16 – Clamped Inductive Waveforms

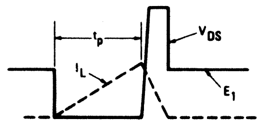


Fig. 17 – Switching Time Test Circuit

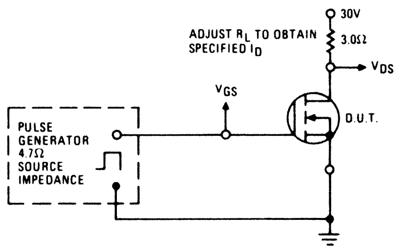
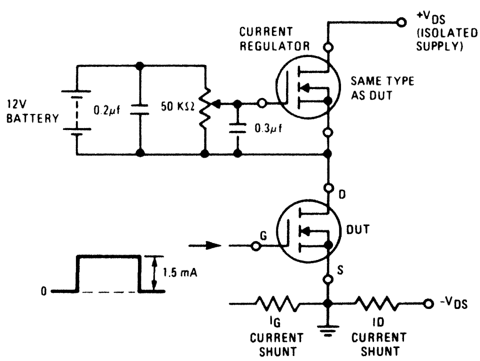


Fig. 18 – Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

200 Volt, 1.5 Ohm
N-Channel

UFN610
UFN611
UFN612
UFN613

FEATURES

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

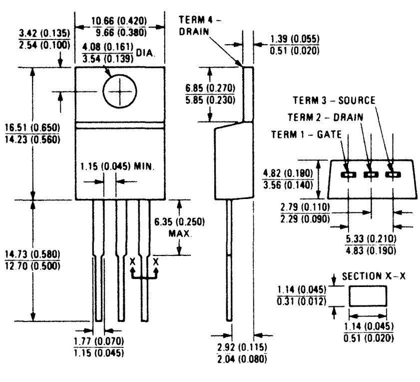
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN610	200V	1.5Ω	2.5A
UFN611	150V	1.5Ω	2.5A
UFN612	200V	2.4Ω	2.0A
UFN613	150V	2.4Ω	2.0A

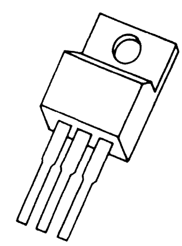
MECHANICAL SPECIFICATIONS

UFN610 UFN611 UFN612 UFN613



Dimensions in Millimeters and (Inches)

TO-220AB



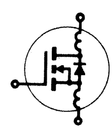
UNITRODE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	UFN610	UFN611	UFN612	UFN613	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	2.5	2.5	2.0	2.0	A
I_D @ T_C = 100°C	Continuous Drain Current	1.5	1.5	1.25	1.25	A
I_{DM}	Pulsed Drain Current ③	10	10	8.0	8.0	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 10	10	8.0	8.0	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

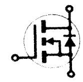
Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFN610 UFN612	200	–	–	V	V_{GS} = 0V
		UFN611 UFN613	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFN610 UFN611	2.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		UFN612 UFN613	2.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFN610 UFN611	–	1.0	1.5	Ω	V_{GS} = 10V, I_D = 1.25A
		UFN612 UFN613	–	1.5	2.4	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.8	1.3	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 1.25A
C_{iss}	Input Capacitance	ALL	–	135	150	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	60	80	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	16	25	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	8.0	15	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 1.25A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	10	15	ns	
t_f	Fall Time	ALL	–	8.0	15	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	5.0	7.5	nC	V_{GS} = 10V, I_D = 3.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	2.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	3.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die. / Modified MOSFET symbol showing the internal device inductances.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.



THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	6.4	K/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN610 UFN611	—	—	2.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFN612 UFN613	—	—	2.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN610 UFN611	—	—	10	A	
		UFN612 UFN613	—	—	8.0	A	
V_{SD}	Diode Forward Voltage ②	UFN610 UFN611	—	—	2.0	V	$T_C = 25°C, I_S = 2.5A, V_{GS} = 0V$
		UFN612 UFN613	—	—	1.8	V	$T_C = 25°C, I_S = 2.0A, V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	290	—	ns	$T_J = 150°C, I_F = 2.5A, dI_F/dt = 100\ A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	2.0	—	μC	$T_J = 150°C, I_F = 2.5A, dI_F/dt = 100\ A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

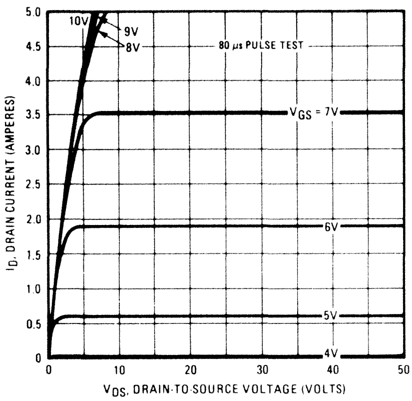


Fig. 2 — Typical Transfer Characteristics

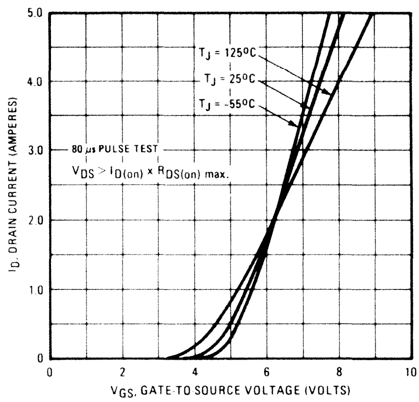


Fig. 3 — Typical Saturation Characteristics

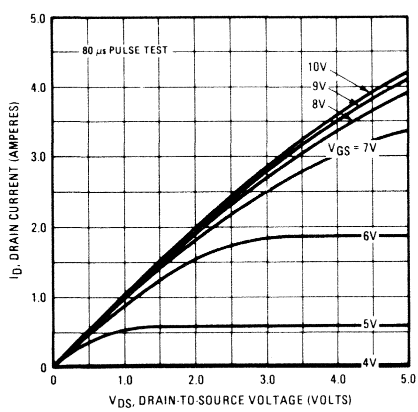


Fig. 4 — Maximum Safe Operating Area

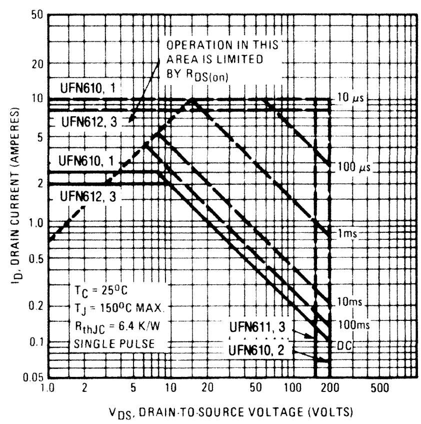


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

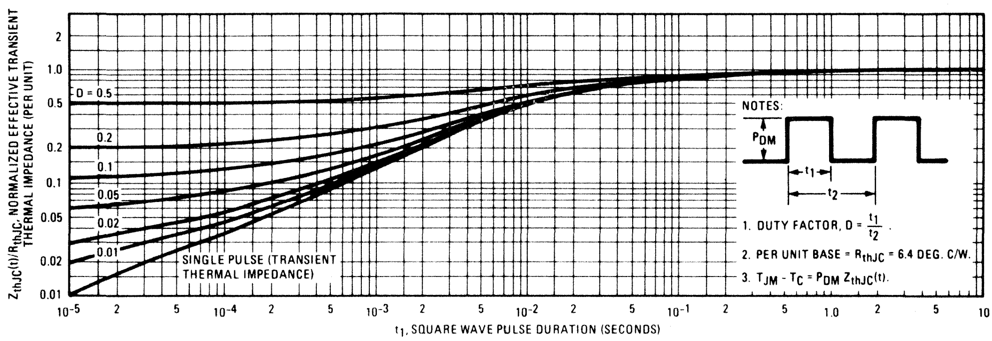


Fig. 6 — Typical Transconductance Vs. Drain Current

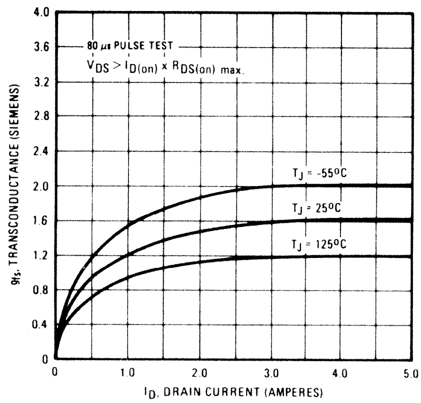


Fig. 7 — Typical Source-Drain Diode Forward Voltage

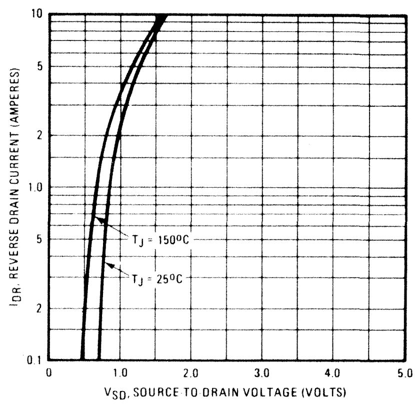


Fig. 8 — Breakdown Voltage Vs. Temperature

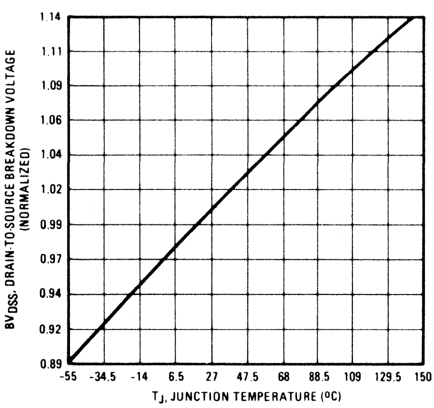


Fig. 9 — Normalized On-Resistance Vs. Temperature

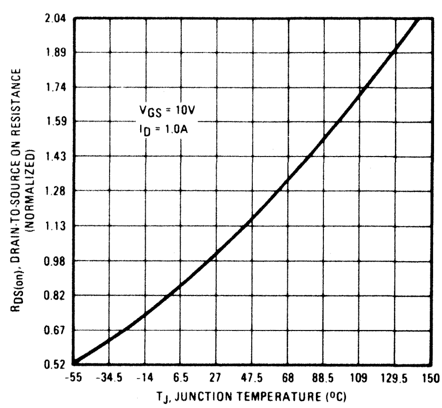


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Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

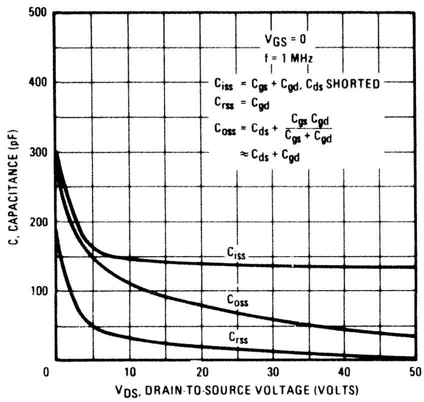

Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

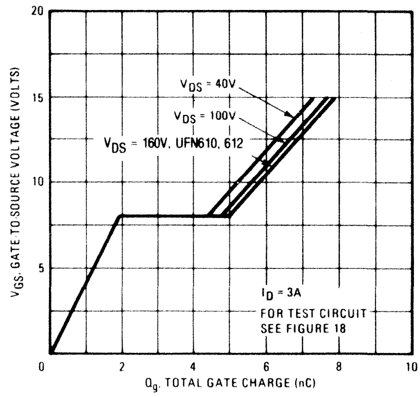

Fig. 12 – Typical On-Resistance Vs. Drain Current

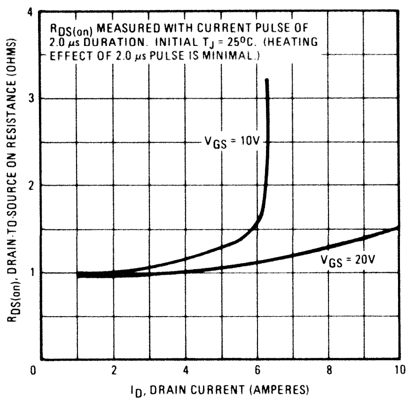

Fig. 13 – Maximum Drain Current Vs. Case Temperature

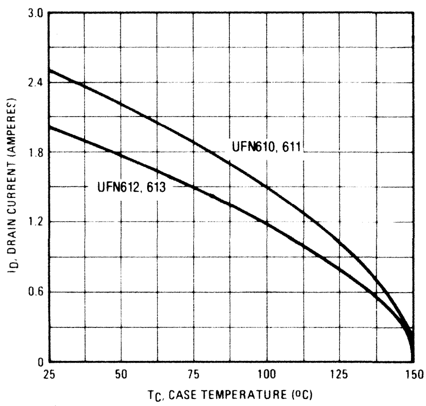

Fig. 14 – Power Vs. Temperature Derating Curve

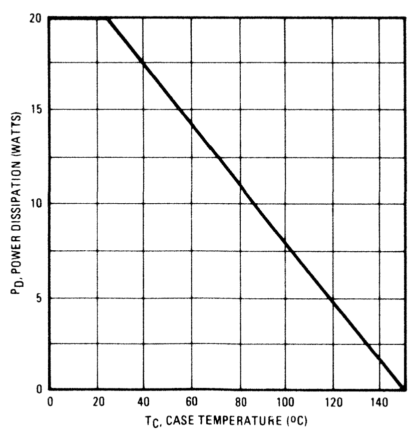

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Fig. 15 — Clamped Inductive Test Circuit

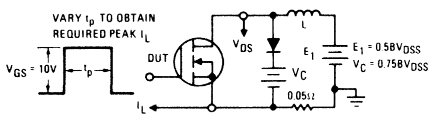


Fig. 16 — Clamped Inductive Waveforms

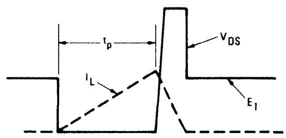


Fig. 17 — Switching Time Test Circuit

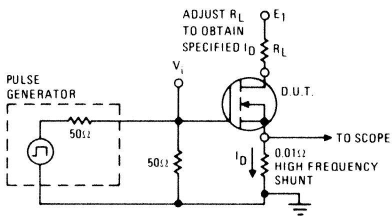
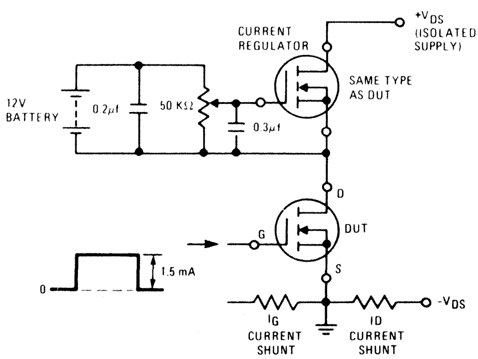


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS
200 Volt, 0.8 Ohm
N-Channel

UFN620
UFN621
UFN622
UFN623

FEATURES
- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

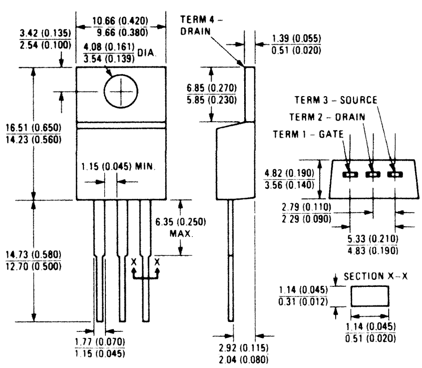
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN620	200V	0.8Ω	5.0A
UFN621	150V	0.8Ω	5.0A
UFN622	200V	1.2Ω	4.0A
UFN623	150V	1.2Ω	4.0A

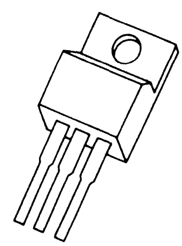
MECHANICAL SPECIFICATIONS

UFN620 UFN621 UFN622 UFN623



Dimensions in Millimeters and (Inches)

TO-220AB



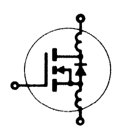
UNITRODE

ABSOLUTE MAXIMUM RATINGS

	Parameter	UFN620	UFN621	UFN622	UFN623	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_D @ T_C = 100°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_{DM}	Pulsed Drain Current ③	20	20	16	16	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 20	20	16	16	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

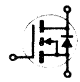
	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFN620 UFN622	200	–	–	V	V_{GS} = 0V
		UFN621 UFN623	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFN620 UFN621	5.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		UFN622 UFN623	4.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFN620 UFN621	–	0.5	0.8	Ω	V_{GS} = 10V, I_D = 2.5A
		UFN622 UFN623	–	0.8	1.2	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.3	2.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 2.5A
C_{iss}	Input Capacitance	ALL	–	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	150	300	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	40	80	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} ≈ 2.5 BV_{DSS}, I_D = 2.5A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	30	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	30	60	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	11	15	nC	V_{GS} = 50V, I_D = 6.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	5.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	6.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die. — Modified MOSFET symbol showing the internal device inductances.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.



THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	K/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN620 UFN621	—	—	5.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFN622 UFN623	—	—	4.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN620 UFN621	—	—	20	A	
		UFN622 UFN623	—	—	16	A	
V_{SD}	Diode Forward Voltage ②	UFN620 UFN621	—	—	1.8	V	$T_C = 25°C$, $I_S = 5.0A$, $V_{GS} = 0V$
		UFN622 UFN623	—	—	1.4	V	$T_C = 25°C$, $I_S = 4.0A$, $V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	350	—	ns	$T_J = 150°C$, $I_F = 5.0A$, $dI_F/dt = 100 A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	2.3	—	μC	$T_J = 150°C$, $I_F = 5.0A$, $dI_F/dt = 100 A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25°C$ to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

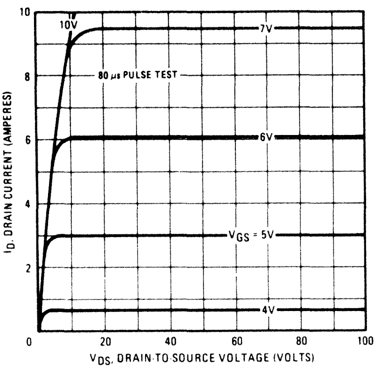


Fig. 2 — Typical Transfer Characteristics

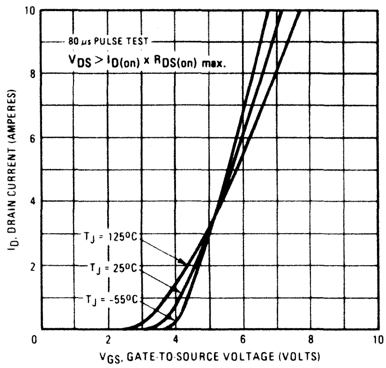


Fig. 3 — Typical Saturation Characteristics

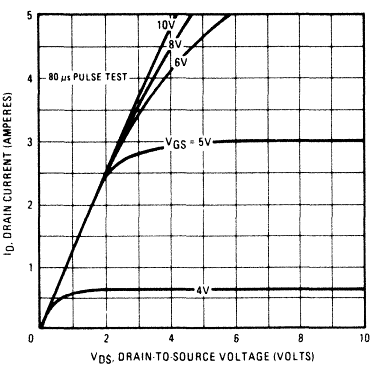


Fig. 4 — Maximum Safe Operating Area

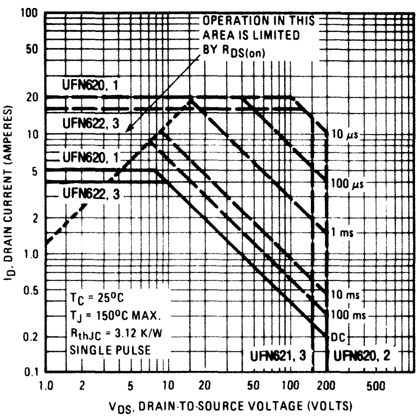


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

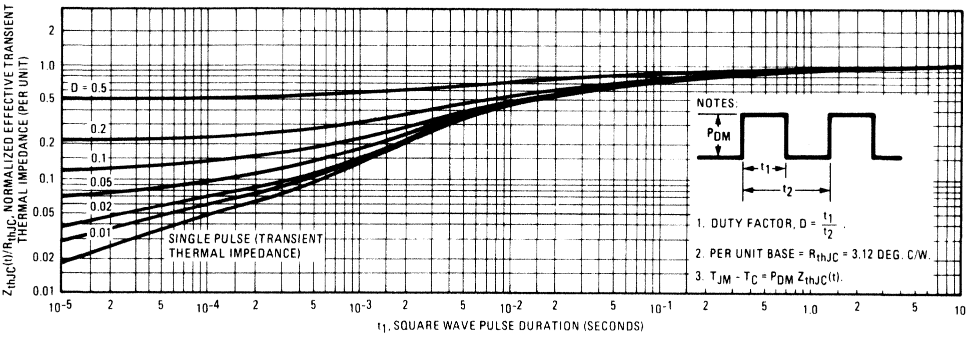


Fig. 6 — Typical Transconductance Vs. Drain Current

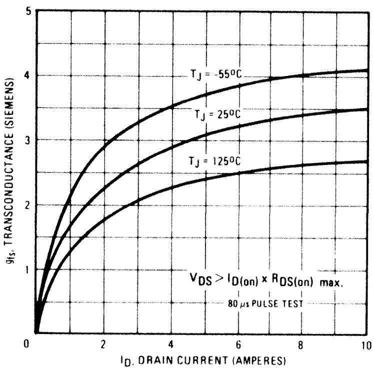


Fig. 7 — Typical Source-Drain Diode Forward Voltage

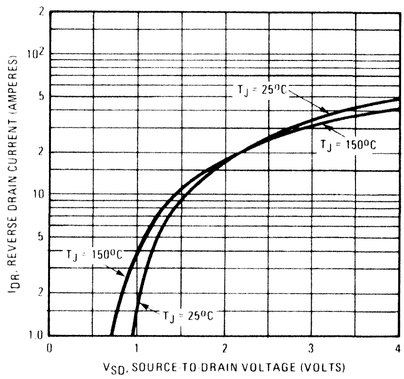


Fig. 8 — Breakdown Voltage Vs. Temperature

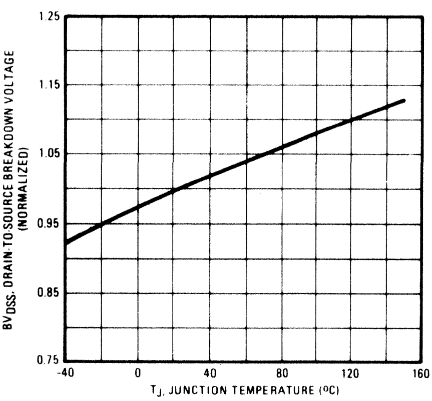


Fig. 9 — Normalized On-Resistance Vs. Temperature

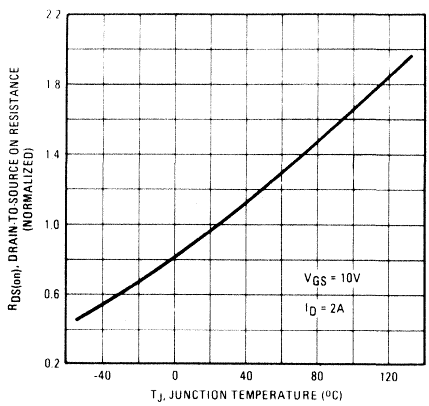


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

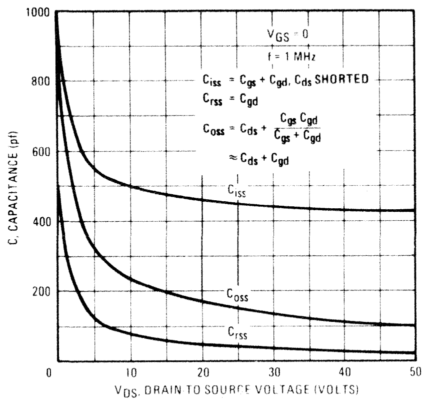


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

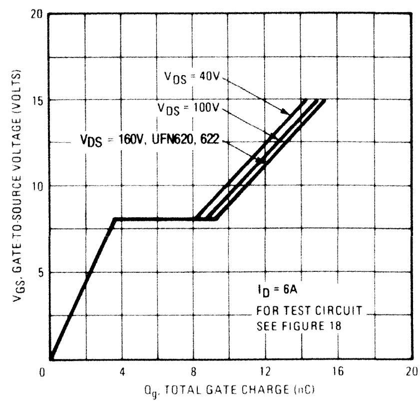


Fig. 12 — Typical On-Resistance Vs. Drain Current

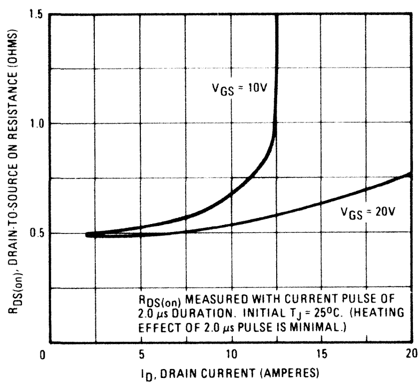


Fig. 13 — Maximum Drain Current Vs. Case Temperature

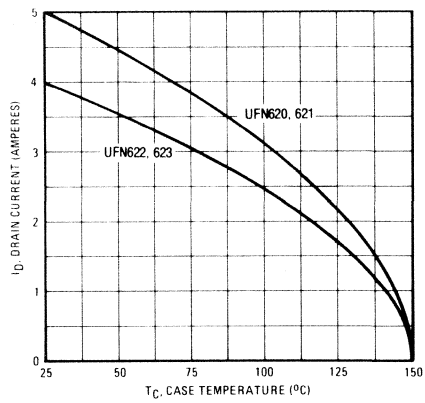


Fig. 14 — Power Vs. Temperature Derating Curve

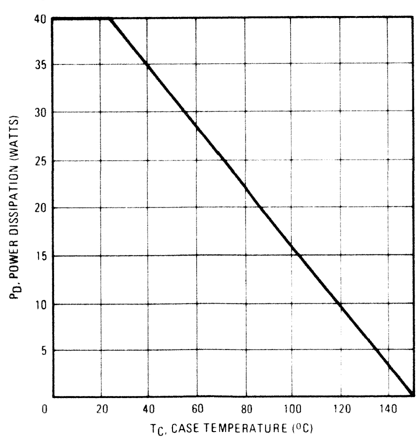


Fig. 15 — Clamped Inductive Test Circuit

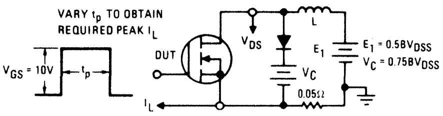


Fig. 16 — Clamped Inductive Waveforms

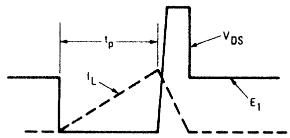


Fig. 17 — Switching Time Test Circuit

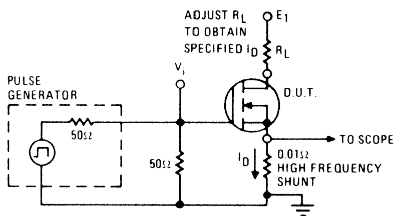
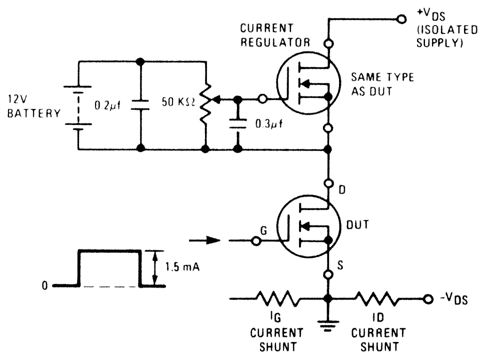


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS
200 Volt, 0.4 Ohm
N-Channel

UFN630
UFN631
UFN632
UFN633

FEATURES
- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION
The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

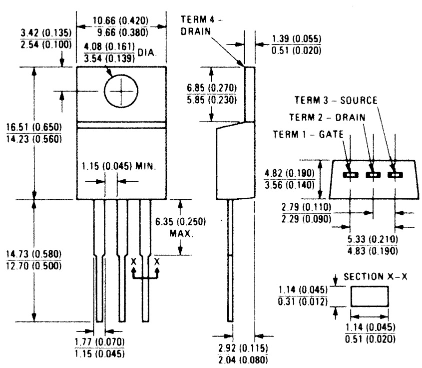
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN630	200V	0.4Ω	9.0A
UFN631	150V	0.4Ω	9.0A
UFN632	200V	0.6Ω	8.0A
UFN633	150V	0.6Ω	8.0A

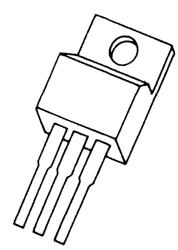
MECHANICAL SPECIFICATIONS

UFN630 UFN631 UFN632 UFN633



Dimensions in Millimeters and (Inches)

TO-220AB

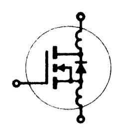


UNITRODE

ABSOLUTE MAXIMUM RATINGS

Parameter		UFN630	UFN631	UFN632	UFN633	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	9.0	9.0	8.0	8.0	A
I_D @ T_C = 100°C	Continuous Drain Current	6.0	6.0	5.0	5.0	A
I_{DM}	Pulsed Drain Current ③	36	36	32	32	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 36	36	32	32	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

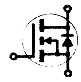
ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFN630 UFN632	200	–	–	V	V_{GS} = 0V
		UFN631 UFN633	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFN630 UFN631	9.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		UFN632 UFN633	8.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFN630 UFN631	–	0.25	0.4	Ω	V_{GS} = 10V, I_D = 5.0A
		UFN632 UFN633	–	0.4	0.6	Ω	
g_{fs}	Forward Transconductance ②	ALL	3.0	4.8	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 5.0A
C_{iss}	Input Capacitance	ALL	–	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	250	450	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	80	150	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} = 90V, I_D = 5.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	50	ns	
t_f	Fall Time	ALL	–	–	40	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	19	30	nC	V_{GS} = 10V, I_D = 12A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	10	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	9.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die. — Modified MOSFET symbol showing the internal device inductances. 
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	K/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN630 UFN631	—	—	9.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFN632 UFN633	—	—	8.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN630 UFN631	—	—	36	A	
		UFN632 UFN633	—	—	32	A	
V_{SD}	Diode Forward Voltage ②	UFN630 UFN631	—	—	2.0	V	$T_C = 25°C, I_S = 9.0A, V_{GS} = 0V$
		UFN632 UFN633	—	—	1.8	V	$T_C = 25°C, I_S = 8.0A, V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	450	—	ns	$T_J = 150°C, I_F = 9.0A, dI_F/dt = 100\ A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	3.0	—	μC	$T_J = 150°C, I_F = 9.0A, dI_F/dt = 100\ A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25°C$ to $150°C$. ② Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

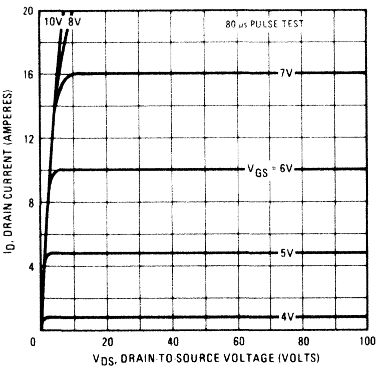


Fig. 2 — Typical Transfer Characteristics

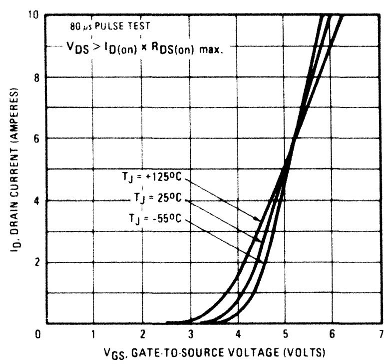


Fig. 3 — Typical Saturation Characteristics

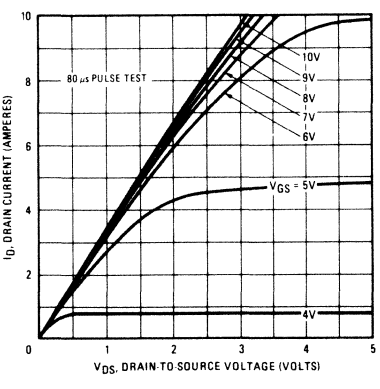


Fig. 4 — Maximum Safe Operating Area

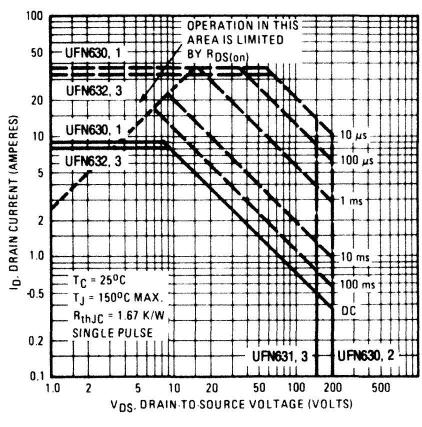


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

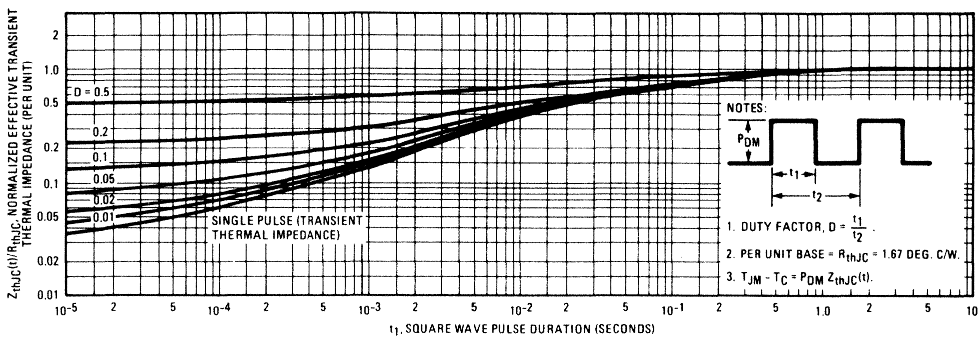


Fig. 6 — Typical Transconductance Vs. Drain Current

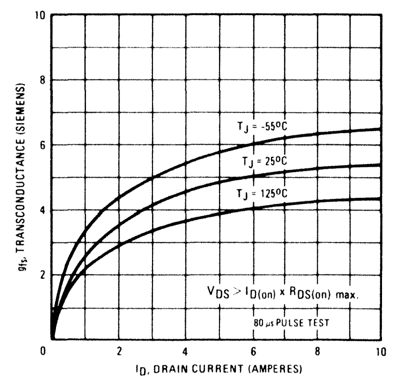


Fig. 7 — Typical Source-Drain Diode Forward Voltage

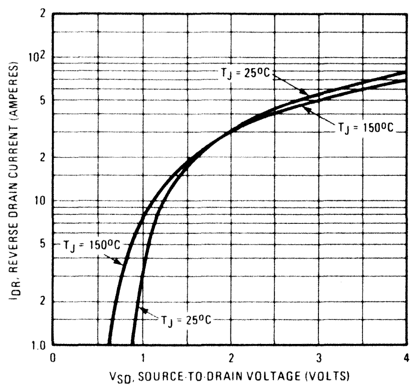


Fig. 8 — Breakdown Voltage Vs. Temperature

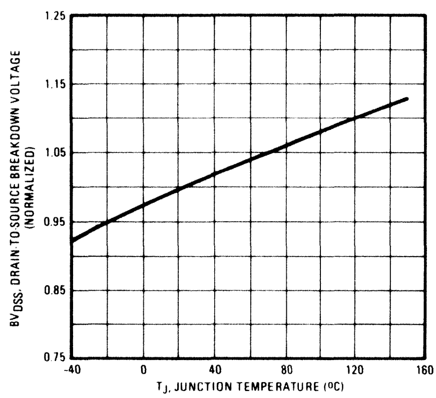


Fig. 9 — Normalized On-Resistance Vs. Temperature

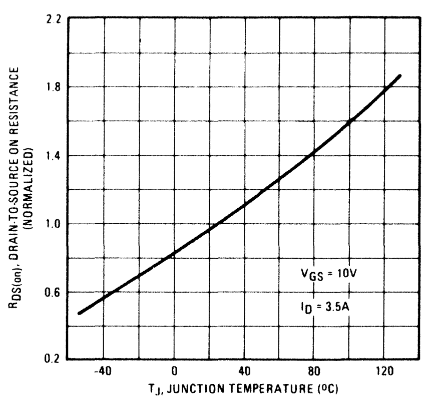


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

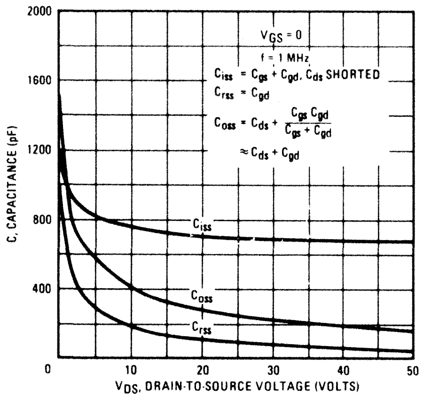


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

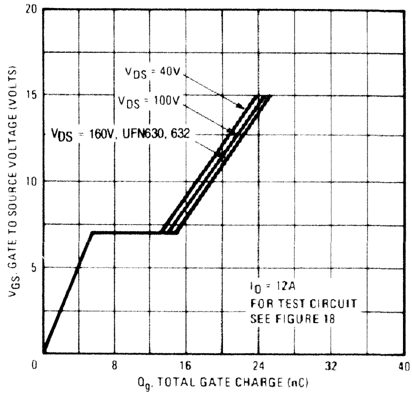


Fig. 12 — Typical On-Resistance Vs. Drain Current

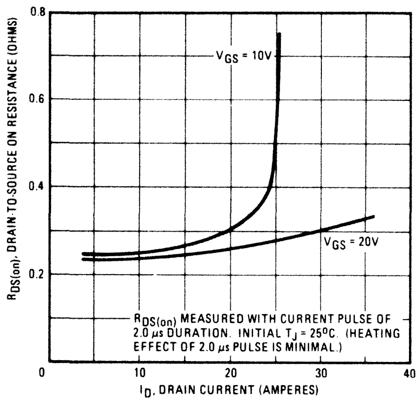


Fig. 13 — Maximum Drain Current Vs. Case Temperature

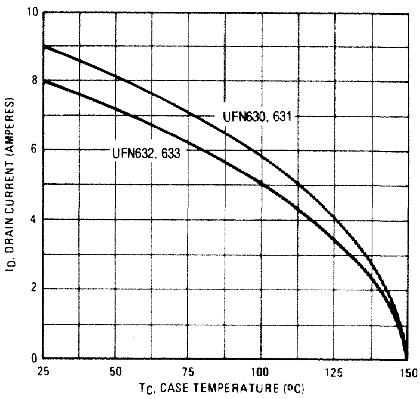


Fig. 14 — Power Vs. Temperature Derating Curve

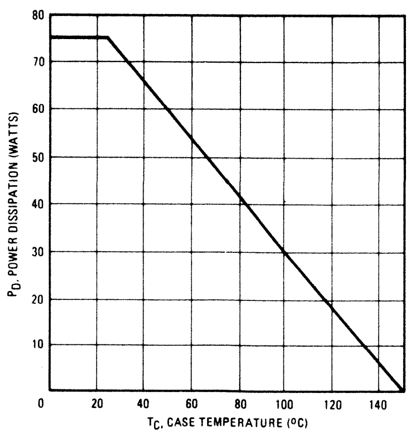


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Fig. 15 — Clamped Inductive Test Circuit

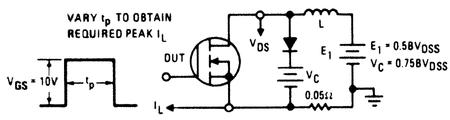


Fig. 16 — Clamped Inductive Waveforms

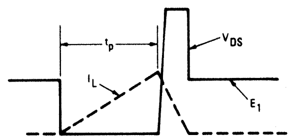


Fig. 17 — Switching Time Test Circuit

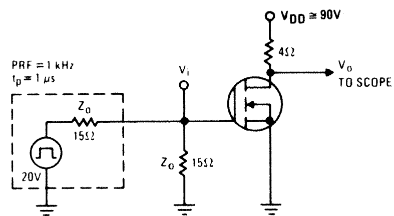
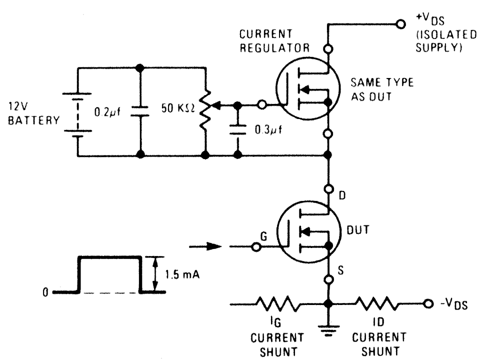


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

200 Volt, 0.2 Ohm
N-Channel

UFN640
UFN641
UFN642
UFN643

FEATURES

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

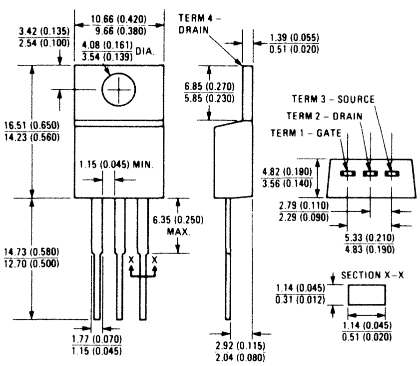
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN640	200V	0.18Ω	18A
UFN641	150V	0.18Ω	18A
UFN642	200V	0.22Ω	16A
UFN643	150V	0.22Ω	16A

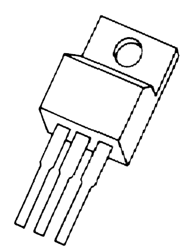
MECHANICAL SPECIFICATIONS

UFN640 UFN641 UFN642 UFN643



Dimensions in Millimeters and (Inches)

TO-220AB



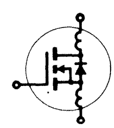
UNITRODE

ABSOLUTE MAXIMUM RATINGS

Parameter		UFN640	UFN641	UFN642	UFN643	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	18	18	16	16	A
I_D @ T_C = 100°C	Continuous Drain Current	11	11	10	10	A
I_{DM}	Pulsed Drain Current ③	72	72	64	64	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 72	72	64	64	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 100				°C
	Lead Temperature	300 (0.064 in. (1.6mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

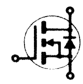
Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFN640 UFN642	200	—	—	V	V_{GS} = 0V
		UFN641 UFN643	150	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFN640 UFN641	18	—	—	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		UFN642 UFN643	16	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFN640 UFN641	—	0.14	0.18	Ω	V_{GS} = 10V, I_D = 10A
		UFN642 UFN643	—	0.20	0.22	Ω	
g_{fs}	Forward Transconductance ②	ALL	6.0	10	—	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 10A
C_{iss}	Input Capacitance	ALL	—	1275	1600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	500	750	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	160	300	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	16	30	ns	V_{DD} = 75V, I_D = 10A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	27	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	40	80	ns	
t_f	Fall Time	ALL	—	31	60	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	43	60	nC	V_{GS} = 10V, I_D = 22A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	16	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	27	—	nC	
L_D	Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die. / Modified MOSFET symbol showing the internal device inductances.
			—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.



THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	—	—	1.0	K/W	
R_{thCS}	Case-to-Sink	ALL	—	1.0	—	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN640 UFN641	–	–	18	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFN642 UFN643	–	–	16	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN640 UFN641	–	–	72	A	
		UFN642 UFN643	–	–	64	A	
V_{SD}	Diode Forward Voltage ②	UFN640 UFN641	–	–	2.0	V	T_C = 25°C, I_S = 18A, V_{GS} = 0V
		UFN642 UFN643	–	–	1.9	V	T_C = 25°C, I_S = 16A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	650	–	ns	T_J = 150°C, I_F = 18A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.1	–	μC	T_J = 150°C, I_F = 18A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

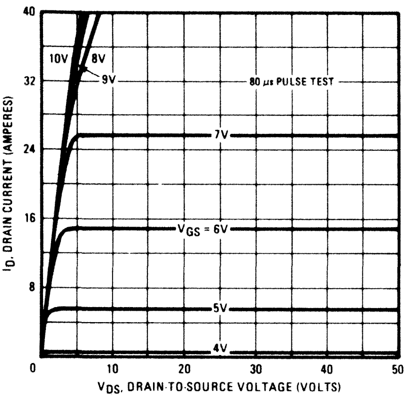


Fig. 2 — Typical Transfer Characteristics

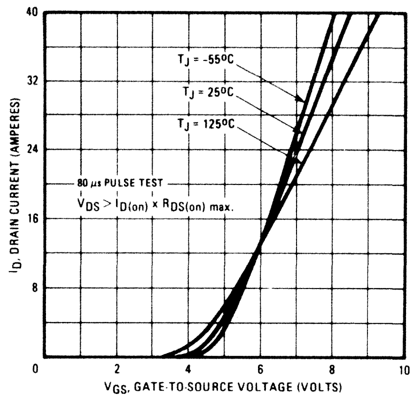


Fig. 3 — Typical Saturation Characteristics

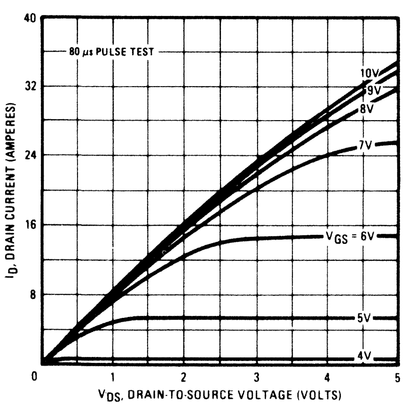


Fig. 4 — Maximum Safe Operating Area

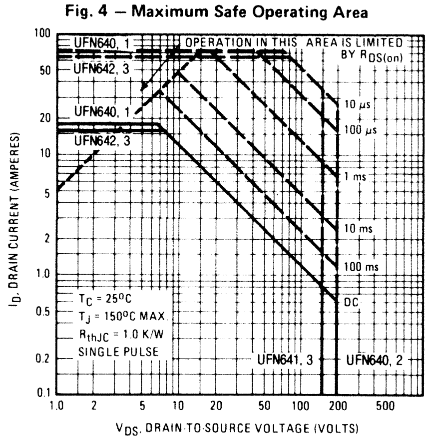


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

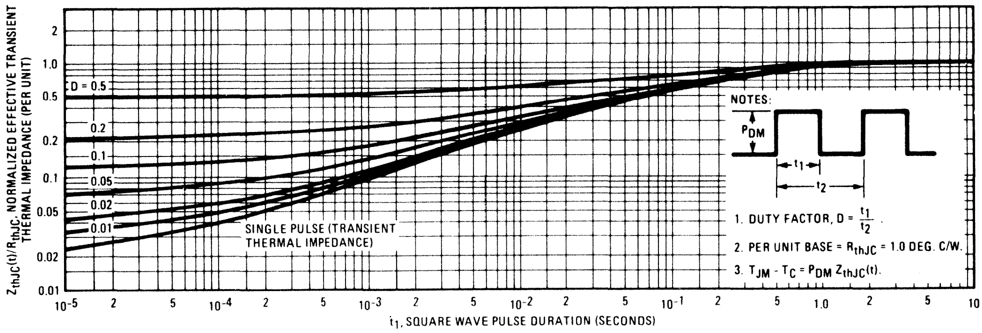


Fig. 6 — Typical Transconductance Vs. Drain Current

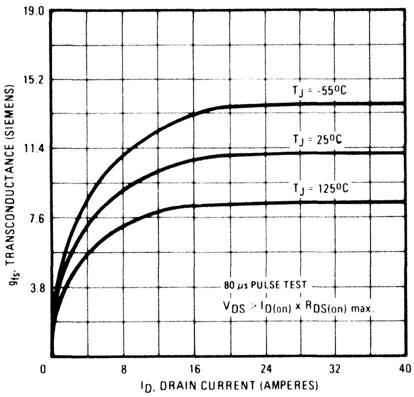


Fig. 7 — Typical Source-Drain Diode Forward Voltage

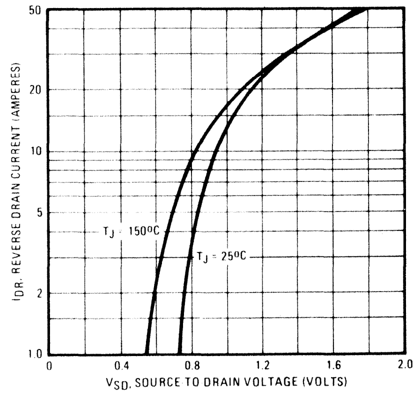


Fig. 8 — Breakdown Voltage Vs. Temperature

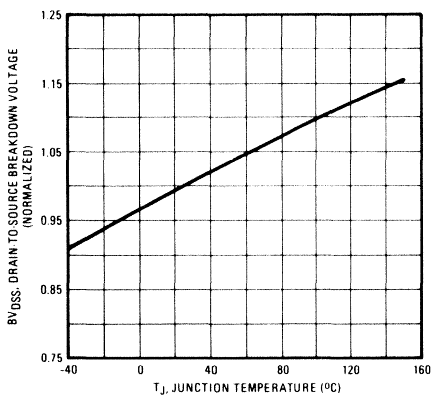


Fig. 9 — Normalized On-Resistance Vs. Temperature

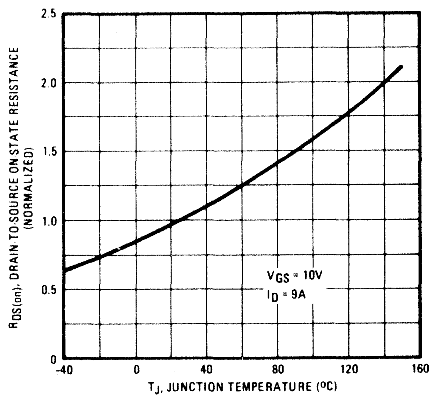


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

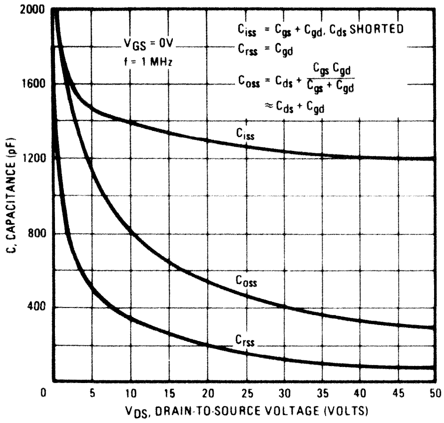


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

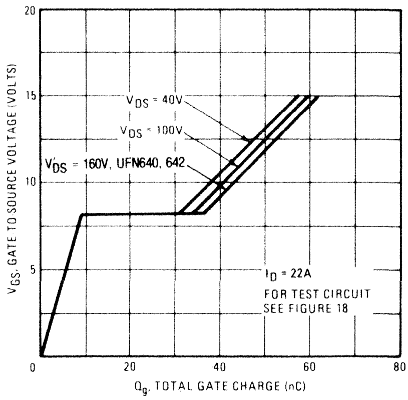


Fig. 12 — Typical On-Resistance Vs. Drain Current

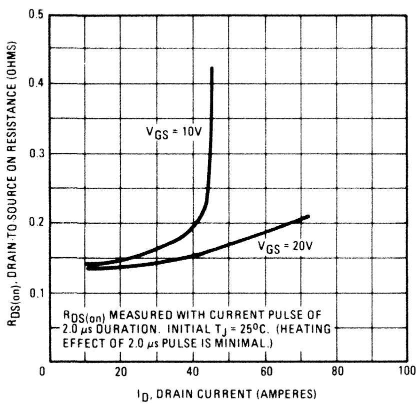


Fig. 13 — Maximum Drain Current Vs. Case Temperature

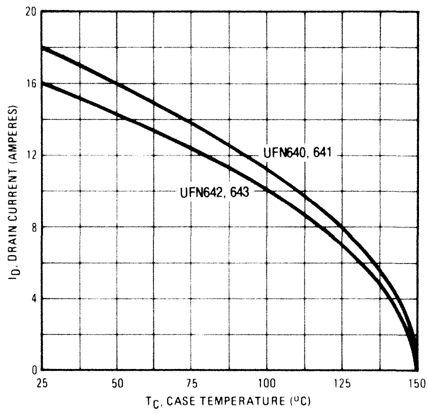


Fig. 14 — Power Vs. Temperature Derating Curve

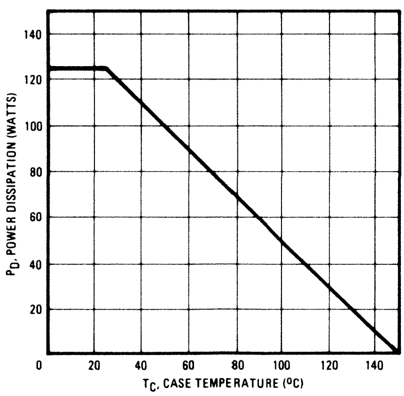


Fig. 15 — Clamped Inductive Test Circuit

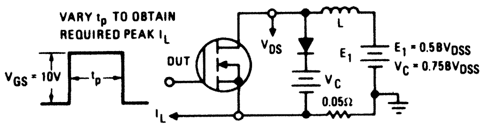


Fig. 16 — Clamped Inductive Waveforms

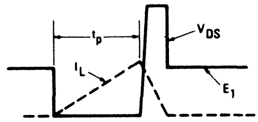


Fig. 17 — Switching Time Test Circuit

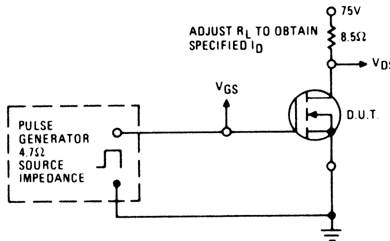
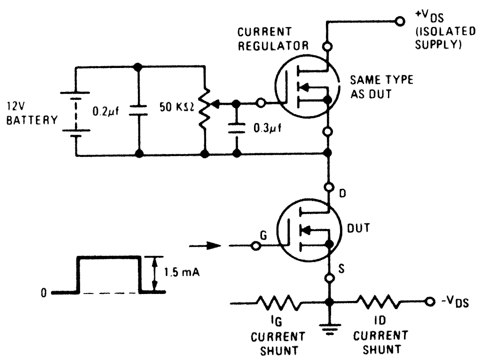


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

400 Volt, 3.6 Ohm
N-Channel

UFN710
UFN711
UFN712
UFN713

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The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

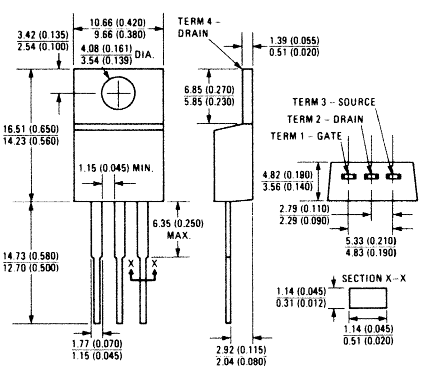
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN710	400V	3.6Ω	1.5A
UFN711	350V	3.6Ω	1.5A
UFN712	400V	5.0Ω	1.3A
UFN713	350V	5.0Ω	1.3A

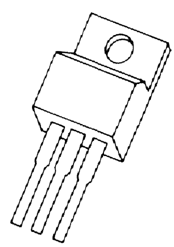
MECHANICAL SPECIFICATIONS

UFN710 UFN711 UFN712 UFN713



Dimensions in Millimeters and (Inches)

TO-220AB



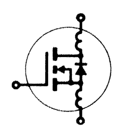
UNITRODE

ABSOLUTE MAXIMUM RATINGS

Parameter		UFN710	UFN711	UFN712	UFN713	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	1.5	1.5	1.3	1.3	A
I_D @ T_C = 100°C	Continuous Drain Current	1.0	1.0	0.8	0.8	A
I_{DM}	Pulsed Drain Current ③	6.0	6.0	5.0	5.0	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 6.0	6.0	5.0	5.0	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

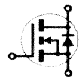
Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFN710 UFN712	400	–	–	V	V_{GS} = 0V
		UFN711 UFN713	350	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFN710 UFN711	1.5	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		UFN712 UFN713	1.3	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFN710 UFN711	–	3.3	3.6	Ω	V_{GS} = 10V, I_D = 0.8A
		UFN712 UFN713	–	3.6	5.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.5	1.2	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 0.8A
C_{iss}	Input Capacitance	ALL	–	135	150	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	35	50	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	8.0	15	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	3.0	10	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 0.8A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	10	20	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	5.0	10	ns	
t_f	Fall Time	ALL	–	8.0	15	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	6.0	7.5	nC	V_{GS} = 10V, I_D = 2.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	3.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	3.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die. — Modified MOSFET symbol showing the internal device inductances.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.



THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	6.4	K/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN710 UFN711	—	—	1.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFN712 UFN713	—	—	1.3	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN710 UFN711	—	—	6.0	A	
		UFN712 UFN713	—	—	5.0	A	
V_{SD}	Diode Forward Voltage ②	UFN710 UFN711	—	—	1.6	V	$T_C = 25°C, I_S = 1.5A, V_{GS} = 0V$
		UFN712 UFN713	—	—	1.5	V	$T_C = 25°C, I_S = 1.3A, V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	380	—	ns	$T_J = 150°C, I_F = 1.5A, dI_F/dt = 100\ A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	2.7	—	μC	$T_J = 150°C, I_F = 1.5A, dI_F/dt = 100\ A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25°C$ to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

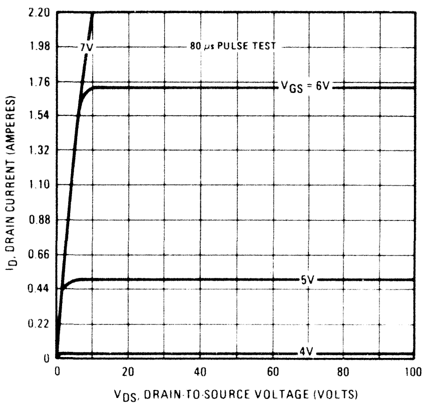


Fig. 2 — Typical Transfer Characteristics

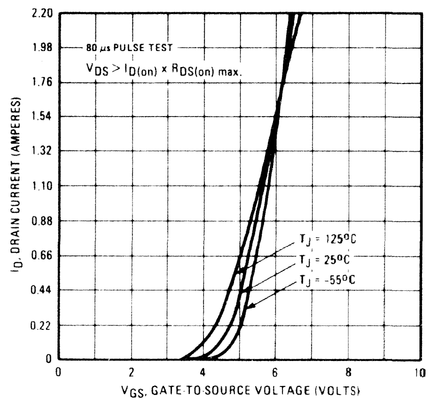


Fig. 3 — Typical Saturation Characteristics

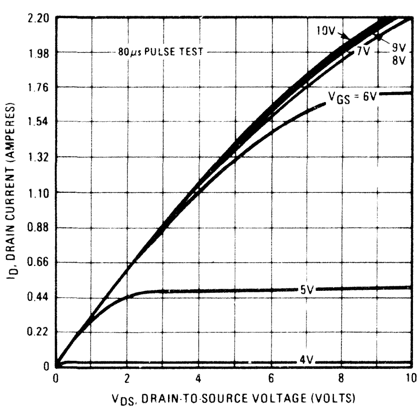


Fig. 4 — Maximum Safe Operating Area

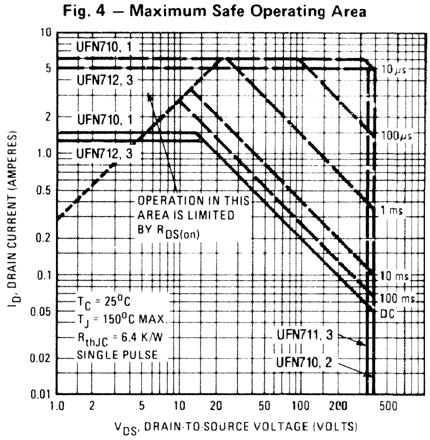


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

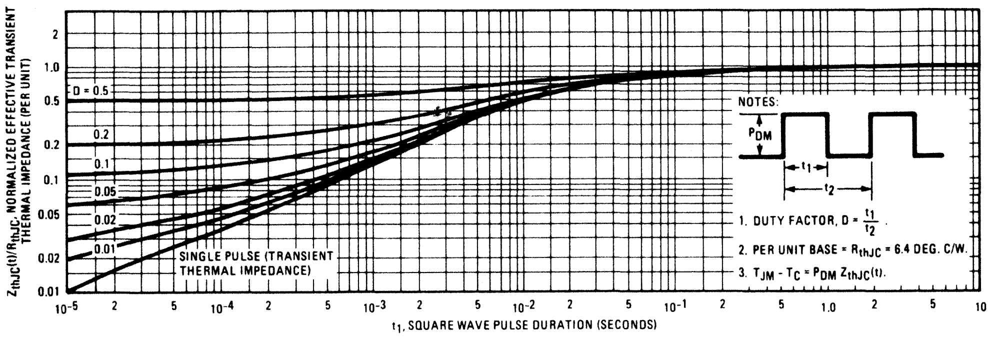


Fig. 6 — Typical Transconductance Vs. Drain Current

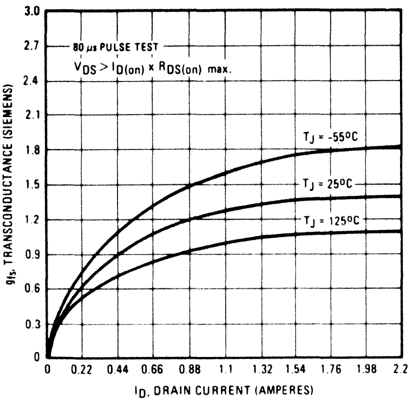


Fig. 7 — Typical Source-Drain Diode Forward Voltage

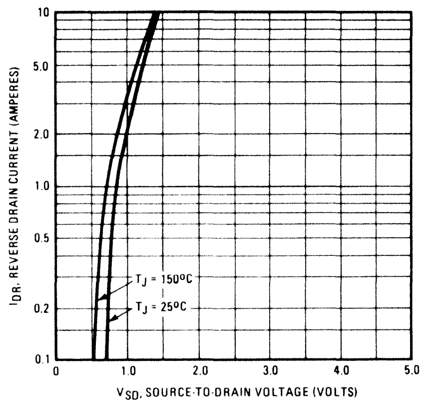


Fig. 8 — Breakdown Voltage Vs. Temperature

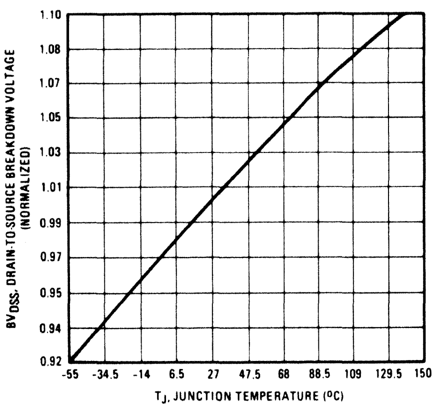


Fig. 9 — Normalized On-Resistance Vs. Temperature

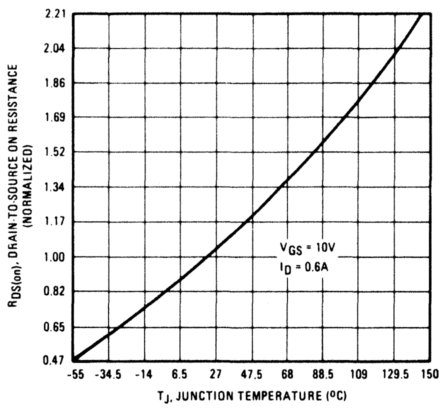


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

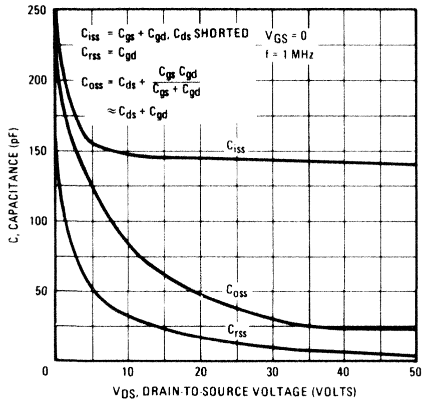


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

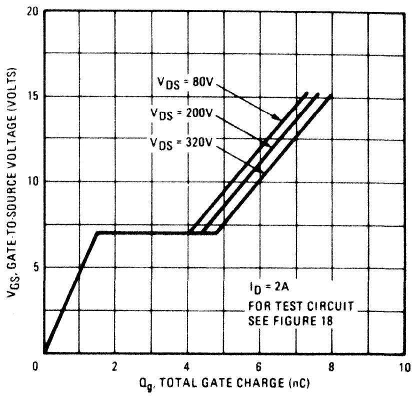


Fig. 12 – Typical On-Resistance Vs. Drain Current

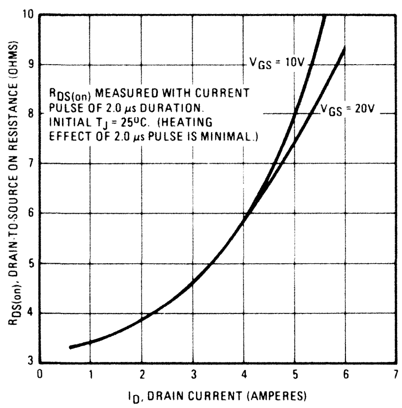


Fig. 13 – Maximum Drain Current Vs. Case Temperature

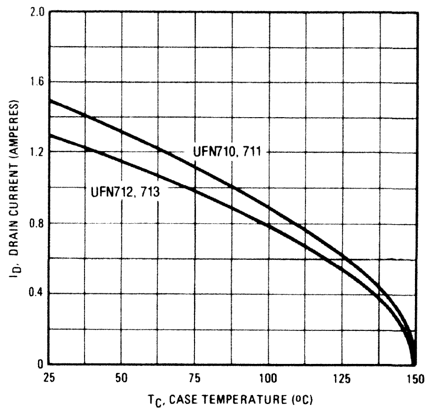


Fig. 14 – Power Vs. Temperature Derating Curve

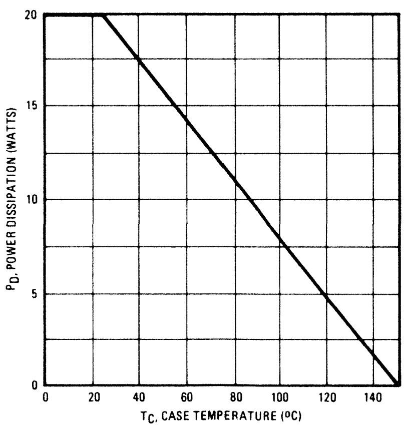


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Fig. 15 — Clamped Inductive Test Circuit

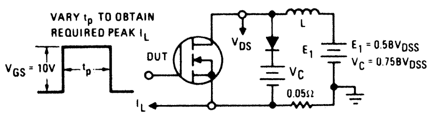


Fig. 16 — Clamped Inductive Waveforms

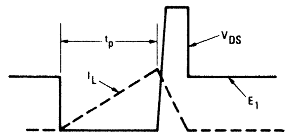


Fig. 17 — Switching Time Test Circuit

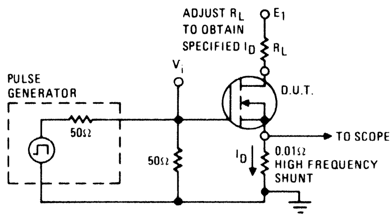
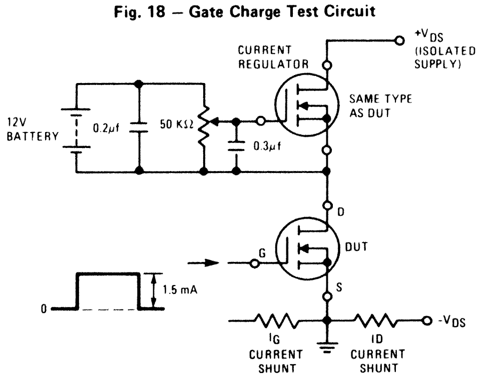


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS
400 Volt, 1.8 Ohm N-Channel

UFN720
UFN721
UFN722
UFN723

FEATURES
- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

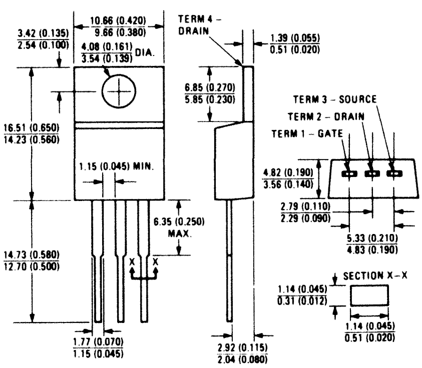
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN720	400V	1.8Ω	3.0A
UFN721	350V	1.8Ω	3.0A
UFN722	400V	2.5Ω	2.5A
UFN723	350V	2.5Ω	2.5A

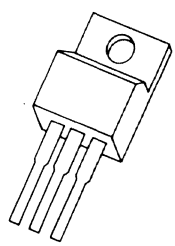
MECHANICAL SPECIFICATIONS

UFN720 UFN721 UFN722 UFN723



Dimensions in Millimeters and (Inches)

TO-220AB

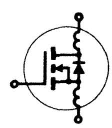


UNITRODE

ABSOLUTE MAXIMUM RATINGS

Parameter		UFN720	UFN721	UFN722	UFN723	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_D @ T_C = 100°C	Continuous Drain Current	2.0	2.0	1.5	1.5	A
I_{DM}	Pulsed Drain Current ③	12	12	10	10	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 12	12	10	10	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

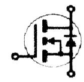
ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFN720 UFN722	400	–	–	V	V_{GS} = 0V
		UFN721 UFN723	350	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFN720 UFN721	3.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)\ max.}$, V_{GS} = 10V
		UFN722 UFN723	2.5	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFN720 UFN721	–	1.5	1.8	Ω	V_{GS} = 10V, I_D = 1.5A
		UFN722 UFN723	–	1.8	2.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	2.0	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)\ max.}$, I_D = 1.5A
C_{iss}	Input Capacitance	ALL	–	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	100	200	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	20	40	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 1.5A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	25	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	25	50	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	12	15	nC	V_{GS} = 10V, I_D = 4.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	6.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	6.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die. — Modified MOSFET symbol showing the internal device inductances. 
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	K/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN720 UFN721	–	–	3.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFN722 UFN723	–	–	2.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN720 UFN721	–	–	12	A	
		UFN722 UFN723	–	–	10	A	
V_{SD}	Diode Forward Voltage ②	UFN720 UFN721	–	–	1.6	V	T_C = 25°C, I_S = 3.0A, V_{GS} = 0V
		UFN722 UFN723	–	–	1.5	V	T_C = 25°C, I_S = 2.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	450	–	ns	T_J = 150°C, I_F = 3.0A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	3.1	–	μC	T_J = 150°C, I_F = 3.0A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

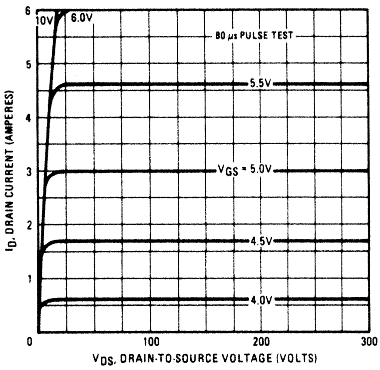


Fig. 2 — Typical Transfer Characteristics

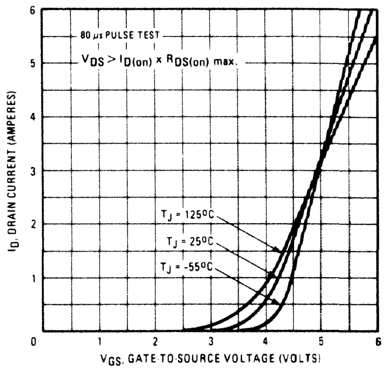


Fig. 3 — Typical Saturation Characteristics

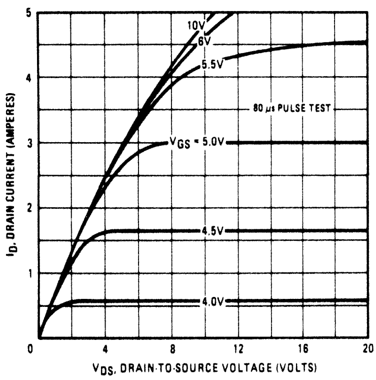


Fig. 4 — Maximum Safe Operating Area

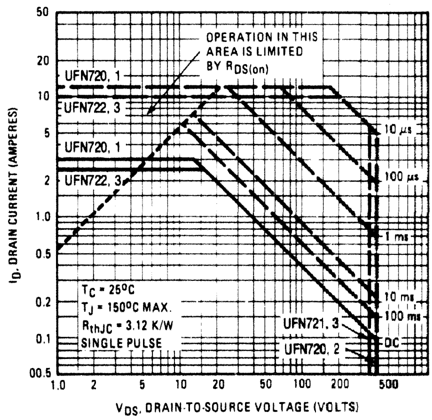


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

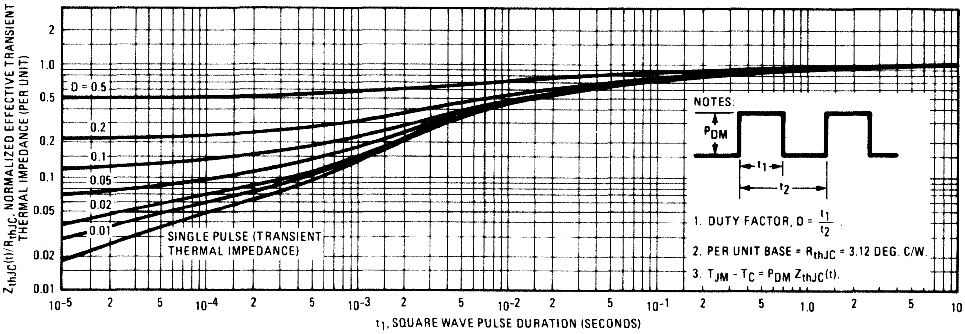


Fig. 6 — Typical Transconductance Vs. Drain Current

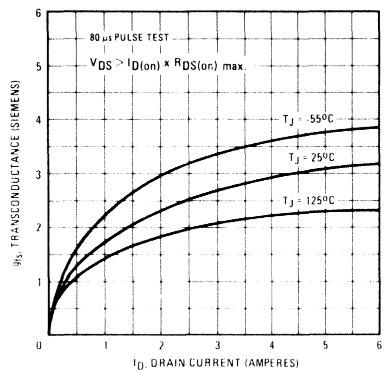


Fig. 7 — Typical Source-Drain Diode Forward Voltage

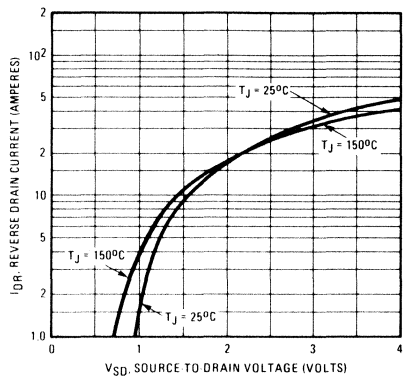


Fig. 8 — Breakdown Voltage Vs. Temperature

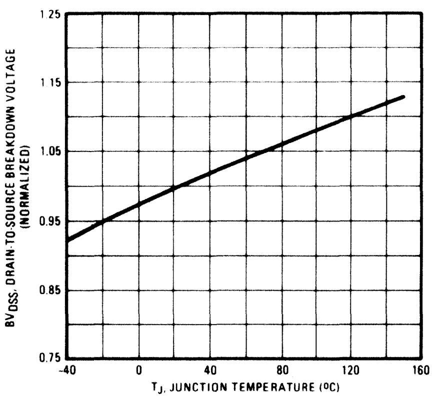


Fig. 9 — Normalized On-Resistance Vs. Temperature

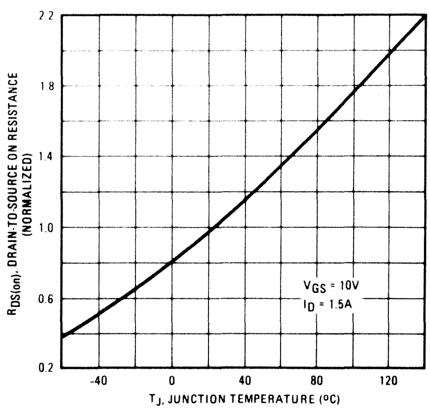


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

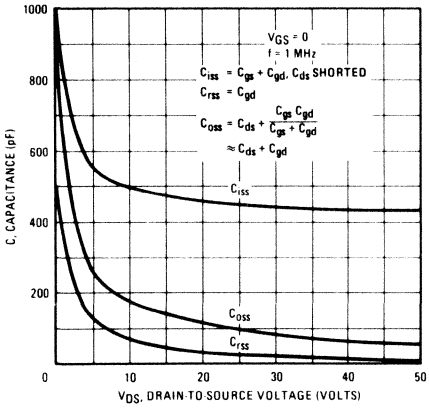


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

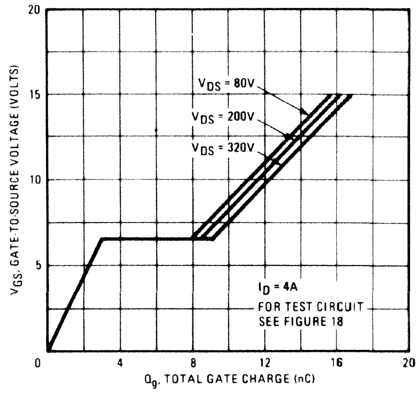


Fig. 12 — Typical On-Resistance Vs. Drain Current

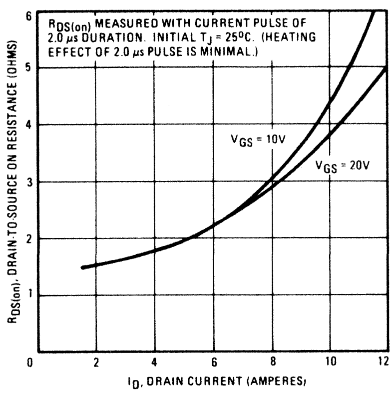


Fig. 13 — Maximum Drain Current Vs. Case Temperature

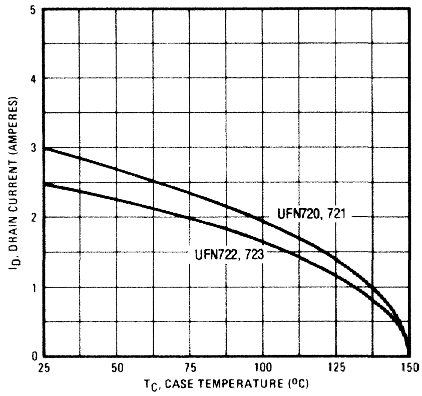


Fig. 14 — Power Vs. Temperature Derating Curve

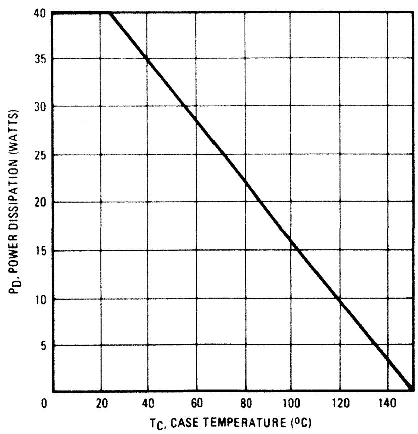


Fig. 15 — Clamped Inductive Test Circuit

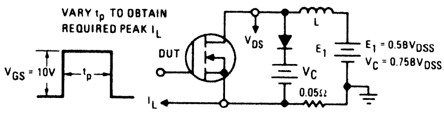


Fig. 16 — Clamped Inductive Waveforms

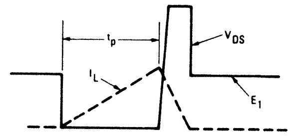


Fig. 17 — Switching Time Test Circuit

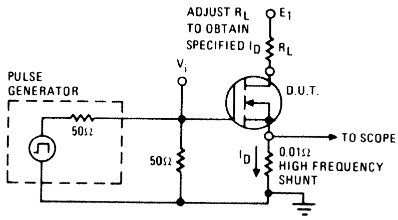
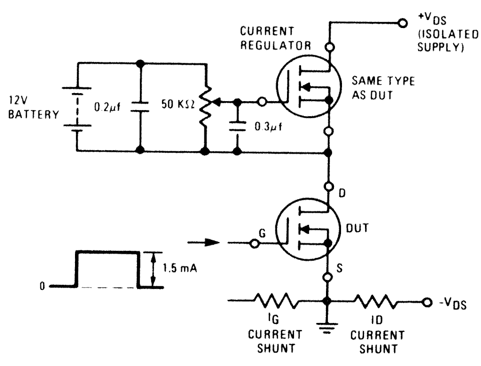


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

400 Volt, 1.0 Ohm
N-Channel

UFN730
UFN731
UFN732
UFN733

FEATURES

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

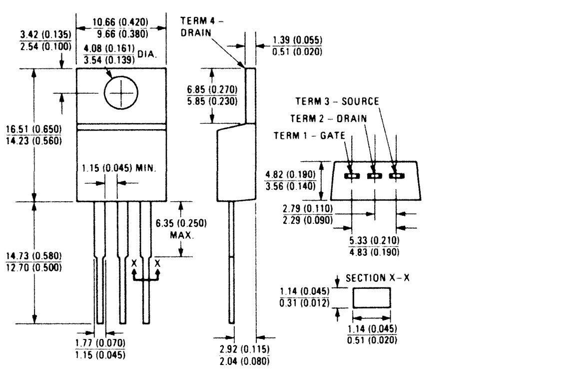
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN730	400V	1.0Ω	5.5A
UFN731	350V	1.0Ω	5.5A
UFN732	400V	1.5Ω	4.5A
UFN733	350V	1.5Ω	4.5A

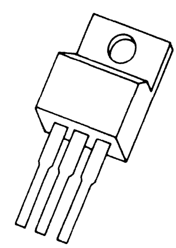
MECHANICAL SPECIFICATIONS

UFN730 UFN731 UFN732 UFN733



Dimensions in Millimeters and (Inches)

TO-220AB



UNITRODE

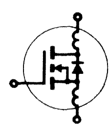
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	UFN730	UFN731	UFN732	UFN733	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	5.5	5.5	4.5	4.5	A
I_D @ T_C = 100°C	Continuous Drain Current	3.5	3.5	3.0	3.0	A
I_{DM}	Pulsed Drain Current ③	22	22	18	18	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 22	22	18	18	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Symbol	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFN730 UFN732	400	–	–	V	V_{GS} = 0V
		UFN731 UFN733	350	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFN730 UFN731	5.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		UFN732 UFN733	4.5	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFN730 UFN731	–	0.8	1.0	Ω	V_{GS} = 10V, I_D = 3.0A
		UFN732 UFN733	–	1.0	1.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	3.0	4.0	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 3.0A
C_{iss}	Input Capacitance	ALL	–	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	150	300	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	40	80	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} = 175V, I_D = 3.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	35	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	55	ns	
t_f	Fall Time	ALL	–	–	35	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	18	30	nC	V_{GS} = 10V, I_D = 7.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	11	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	7.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

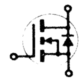
Modified MOSFET symbol showing the internal device inductances.



THERMAL RESISTANCE

Symbol	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
R_{thJC}	Junction-to-Case	ALL	–	–	1.67	K/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN730 UFN731	—	—	5.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFN732 UFN733	—	—	4.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN730 UFN731	—	—	22	A	
		UFN732 UFN733	—	—	18	A	
V_{SD}	Diode Forward Voltage ②	UFN730 UFN731	—	—	1.6	V	$T_C = 25°C, I_S = 5.5A, V_{GS} = 0V$
		UFN732 UFN733	—	—	1.5	V	$T_C = 25°C, I_S = 4.5A, V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	600	—	ns	$T_J = 150°C, I_F = 5.5A, dI_F/dt = 100\ A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	4.0	—	μC	$T_J = 150°C, I_F = 5.5A, dI_F/dt = 100\ A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25°C$ to $150°C$. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

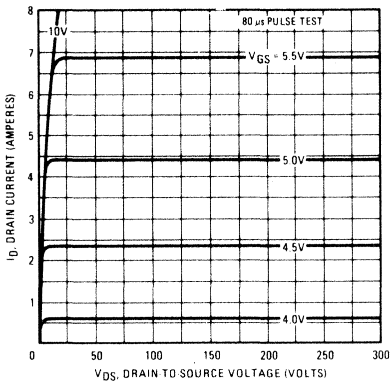


Fig. 2 — Typical Transfer Characteristics

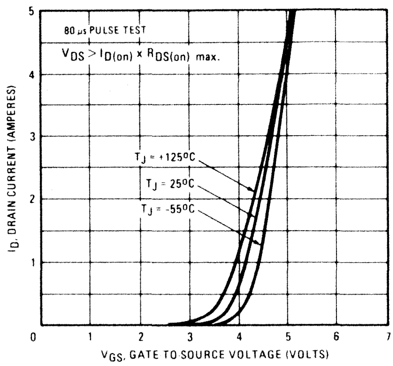


Fig. 3 — Typical Saturation Characteristics

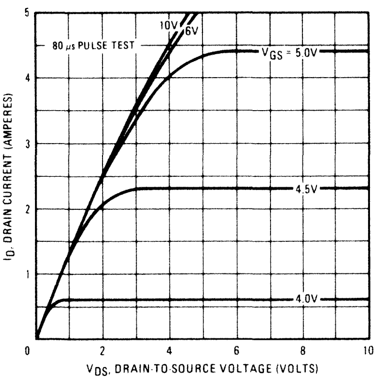


Fig. 4 — Maximum Safe Operating Area

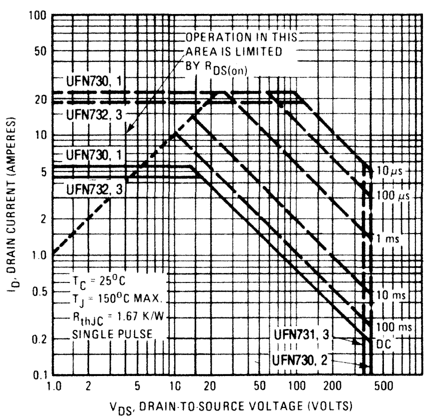


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

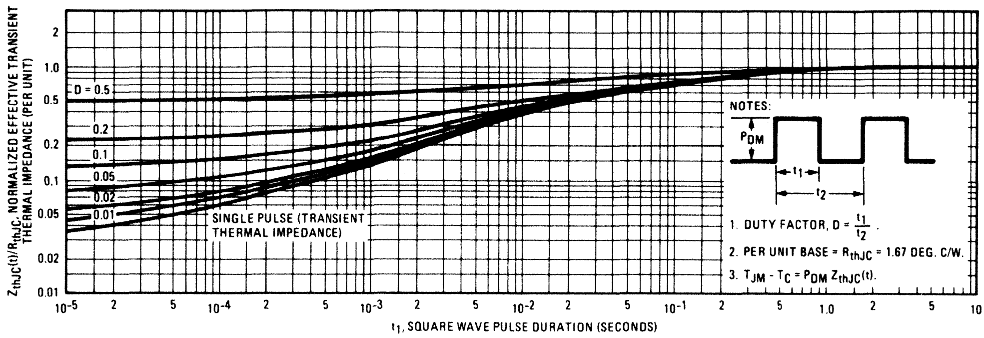


Fig. 6 — Typical Transconductance Vs. Drain Current

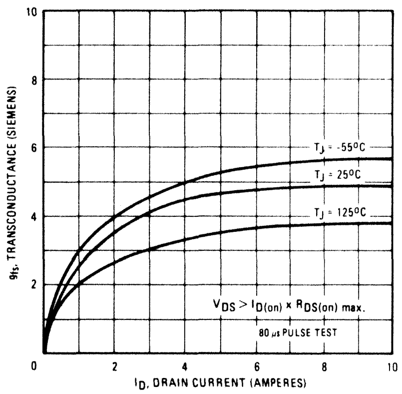


Fig. 7 — Typical Source-Drain Diode Forward Voltage

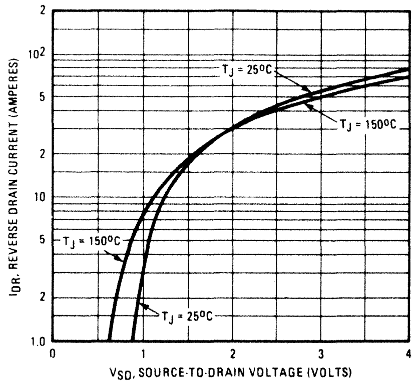


Fig. 8 — Breakdown Voltage Vs. Temperature

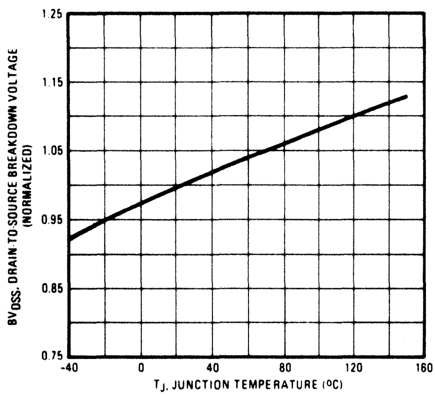


Fig. 9 — Normalized On-Resistance Vs. Temperature

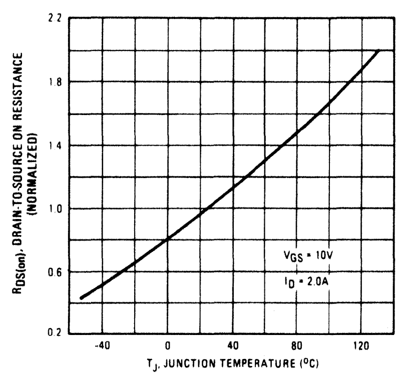


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Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

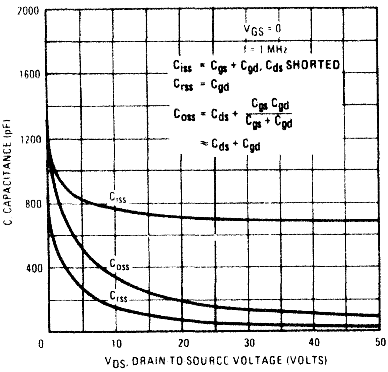


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

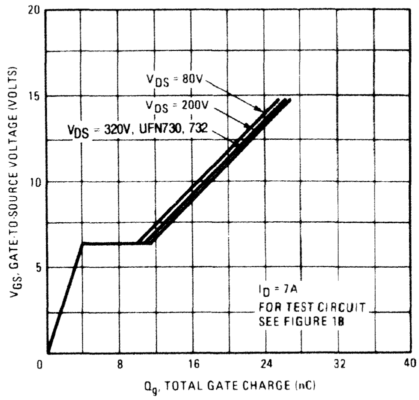


Fig. 12 — Typical On-Resistance Vs. Drain Current

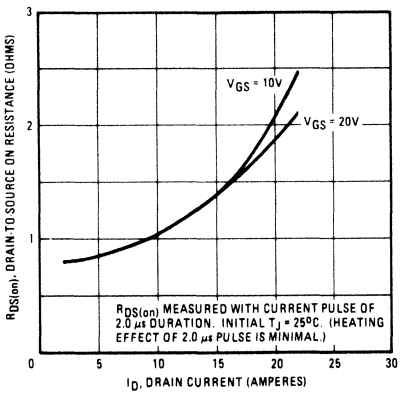


Fig. 13 — Maximum Drain Current Vs. Case Temperature

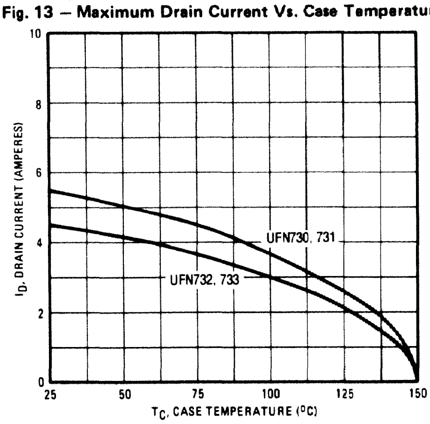


Fig. 14 — Power Vs. Temperature Derating Curve

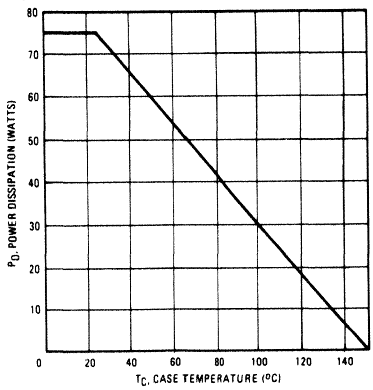


Fig. 15 – Clamped Inductive Test Circuit

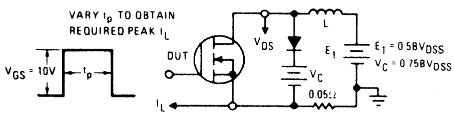


Fig. 16 – Clamped Inductive Waveforms

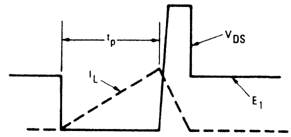


Fig. 17 – Switching Time Test Circuit

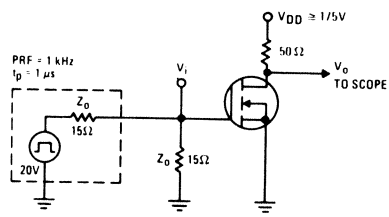
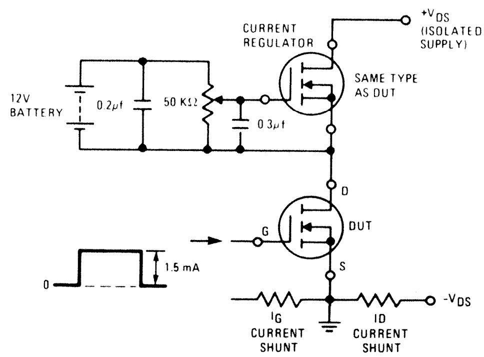


Fig. 18 – Gate Charge Test Circuit



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POWER MOSFET TRANSISTORS

400 Volt, 0.55 Ohm
N-Channel

UFN740
UFN741
UFN742
UFN743

FEATURES

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

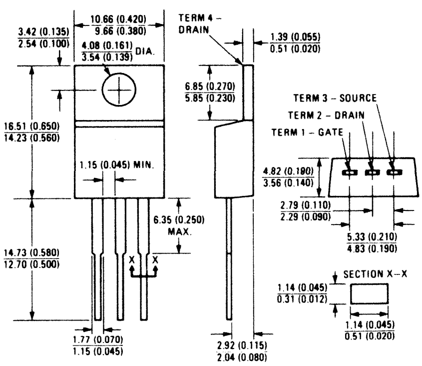
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN740	400V	0.55Ω	10A
UFN741	350V	0.55Ω	10A
UFN742	400V	0.80Ω	8.0A
UFN743	350V	0.80Ω	8.0A

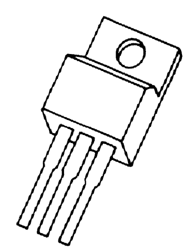
MECHANICAL SPECIFICATIONS

UFN740 UFN741 UFN742 UFN743



Dimensions in Millimeters and (Inches)

TO-220AB

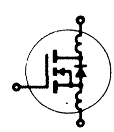


UNITRODE

ABSOLUTE MAXIMUM RATINGS

Parameter		UFN740	UFN741	UFN742	UFN743	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	10	10	8.0	8.0	A
I_D @ T_C = 100°C	Continuous Drain Current	6.0	6.0	5.0	5.0	A
I_{DM}	Pulsed Drain Current ③	40	40	32	32	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 40	40	32	32	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions	
BV_{DSS}	Drain - Source Breakdown Voltage	UFN740 UFN742	400	–	–	V	V_{GS} = 0V	
		UFN741 UFN743	350	–	–	V	I_D = 250μA	
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA	
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V	
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V	
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V	
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C	
$I_{D(on)}$	On-State Drain Current ②	UFN740 UFN741	10	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V	
		UFN742 UFN743	8.0	–	–	A		
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFN740 UFN741	–	0.47	0.55	Ω	V_{GS} = 10V, I_D = 5.0A	
		UFN742 UFN743	–	.68	.80	Ω		
g_{fs}	Forward Transconductance ②	ALL	4.0	7.0	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 5.0A	
C_{iss}	Input Capacitance	ALL	–	1250	1600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10	
C_{oss}	Output Capacitance	ALL	–	300	450	pF		
C_{rss}	Reverse Transfer Capacitance	ALL	–	80	150	pF		
$t_{d(on)}$	Turn-On Delay Time	ALL	–	17	35	ns	V_{DD} = 175V, I_D = 5.0A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t_r	Rise Time	ALL	–	5.0	15	ns		
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	45	90	ns		
t_f	Fall Time	ALL	–	16	35	ns		
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	41	60	nC	V_{GS} = 10V, I_D = 12A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q_{gs}	Gate-Source Charge	ALL	–	18	–	nC		
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	23	–	nC		
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.	Modified MOSFET symbol showing the internal device inductances. 
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.	
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.	

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	1.0	K/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

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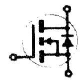
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN740 UFN741	–	–	10	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFN742 UFN743	–	–	8.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN740 UFN741	–	–	40	A	
		UFN742 UFN743	–	–	32	A	
V_{SD}	Diode Forward Voltage ②	UFN740 UFN741	–	–	2.0	V	T_C = 25°C, I_S = 10A, V_{GS} = 0V
		UFN742 UFN743	–	–	1.9	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	800	–	ns	T_J = 150°C, I_F = 10A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	5.7	–	μC	T_J = 150°C, I_F = 10A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

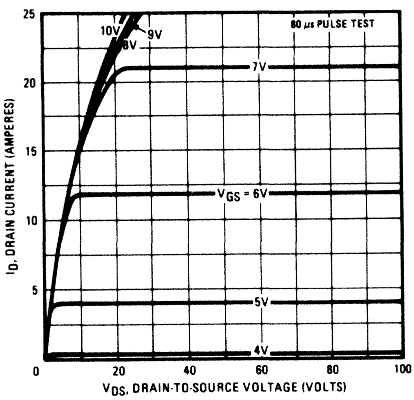


Fig. 2 — Typical Transfer Characteristics

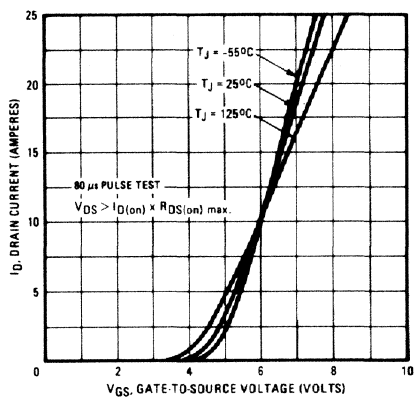


Fig. 3 — Typical Saturation Characteristics

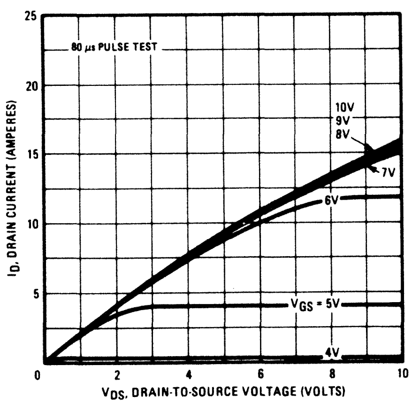


Fig. 4 — Maximum Safe Operating Area

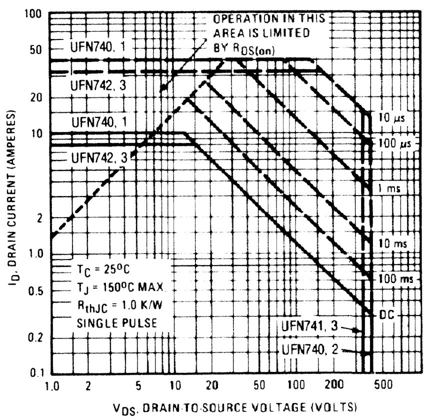


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

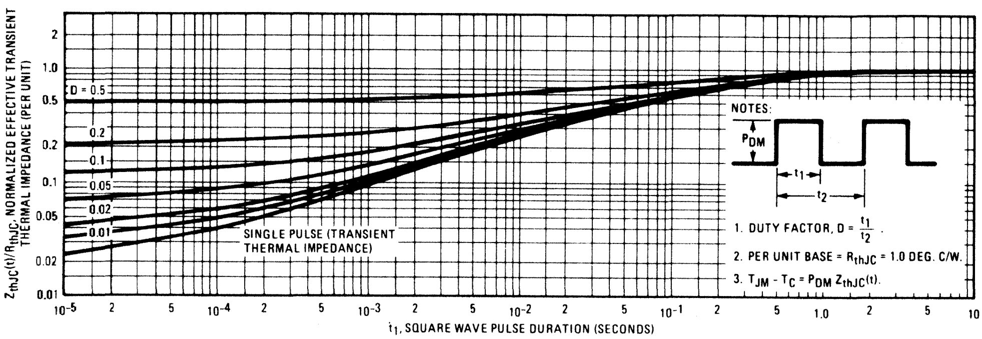


Fig. 6 — Typical Transconductance Vs. Drain Current

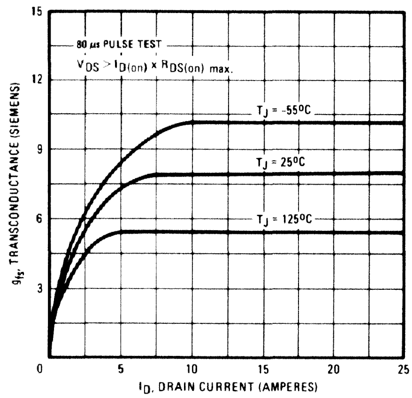


Fig. 7 — Typical Source-Drain Diode Forward Voltage

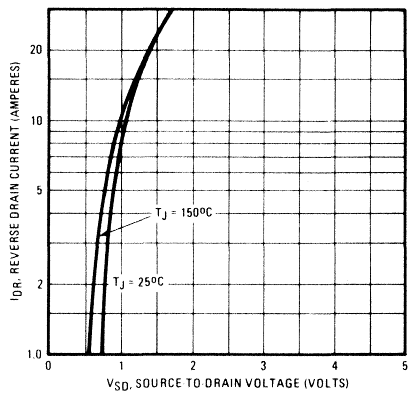


Fig. 8 — Breakdown Voltage Vs. Temperature

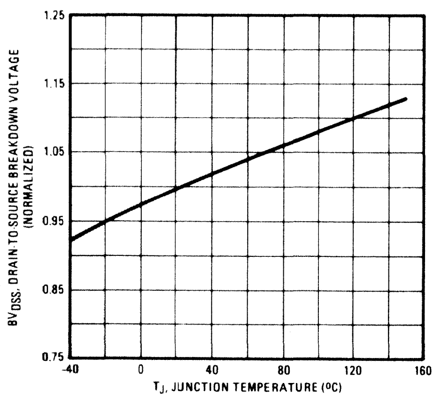


Fig. 9 — Normalized On-Resistance Vs. Temperature

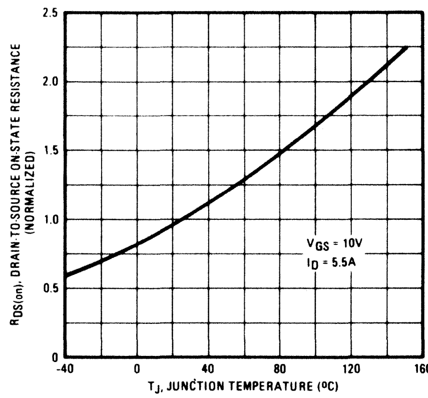


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Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

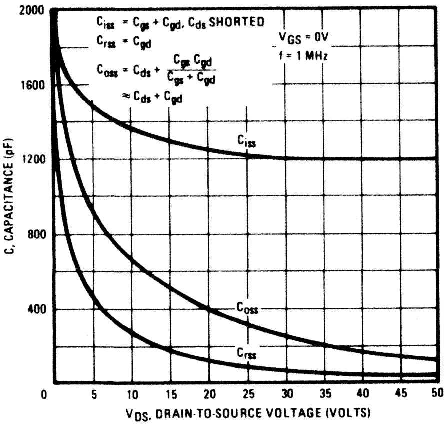


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

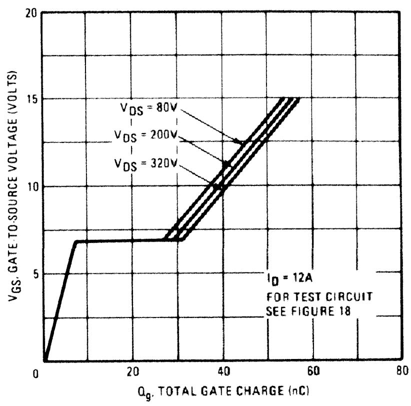


Fig. 12 — Typical On-Resistance Vs. Drain Current

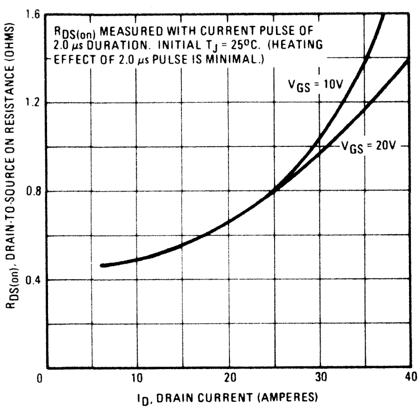


Fig. 13 — Maximum Drain Current Vs. Case Temperature

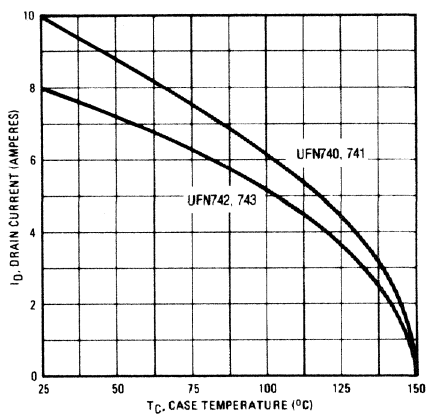


Fig. 14 — Power Vs. Temperature Derating Curve

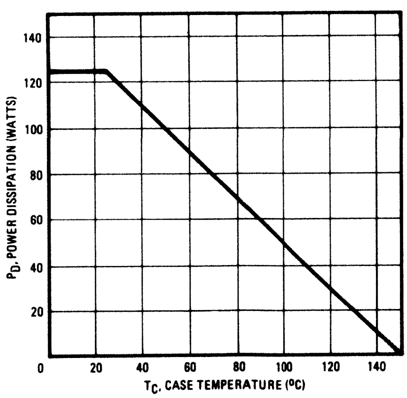


Fig. 15 — Clamped Inductive Test Circuit

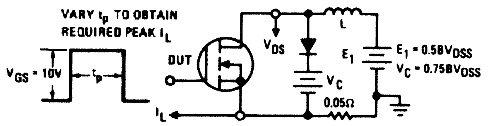


Fig. 16 — Clamped Inductive Waveforms

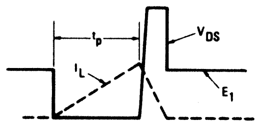


Fig. 17 — Switching Time Test Circuit

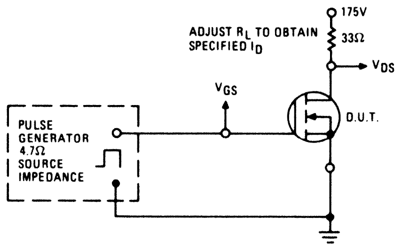
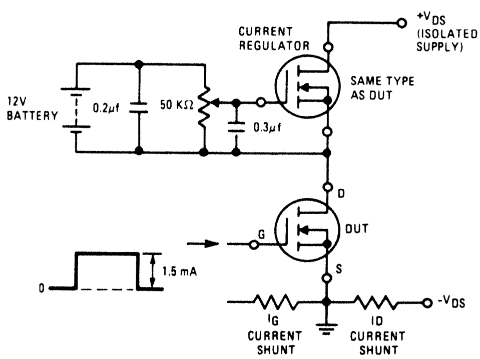


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS

500 Volt, 3.0 Ohm
N-Channel

UFN820
UFN821
UFN822
UFN823

FEATURES
- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

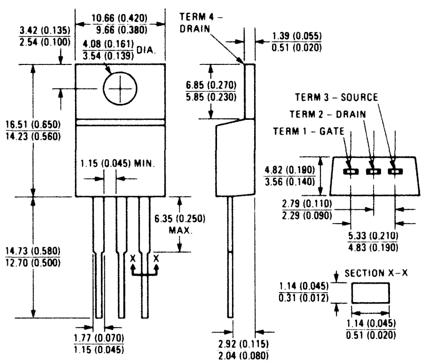
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN820	500V	3.0Ω	2.5A
UFN821	450V	3.0Ω	2.5A
UFN822	500V	4.0Ω	2.0A
UFN823	450V	4.0Ω	2.0A

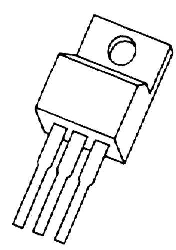
MECHANICAL SPECIFICATIONS

UFN820 UFN821 UFN822 UFN823



Dimensions in Millimeters and (Inches)

TO-220AB

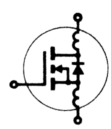


UNITRODE

ABSOLUTE MAXIMUM RATINGS

Parameter		UFN820	UFN821	UFN822	UFN823	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	2.5	2.5	2.0	2.0	A
I_D @ T_C = 100°C	Continuous Drain Current	1.5	1.5	1.0	1.0	A
I_{DM}	Pulsed Drain Current ③	10	10	8.0	8.0	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 10	10	8.0	8.0	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

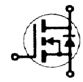
ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFN820 UFN822	500	–	–	V	V_{GS} = 0V
		UFN821 UFN823	450	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFN820 UFN821	2.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		UFN822 UFN823	2.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFN820 UFN821	–	2.5	3.0	Ω	V_{GS} = 10V, I_D = 1.0A
		UFN822 UFN823	–	3.0	4.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	1.75	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 1.0A
C_{iss}	Input Capacitance	ALL	–	300	400	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	75	150	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	20	40	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	30	60	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 1.0A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	25	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	30	60	ns	
t_f	Fall Time	ALL	–	15	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	11	15	nC	V_{GS} = 10V, I_D = 3.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	5.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	6.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die. — Modified MOSFET symbol showing the internal device inductances. 
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	K/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN820 UFN821	–	–	2.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFN822 UFN823	–	–	2.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN820 UFN821	–	–	10	A	
		UFN822 UFN823	–	–	8.0	A	
V_{SD}	Diode Forward Voltage ②	UFN820 UFN821	–	–	1.6	V	$T_C = 25°C, I_S = 2.5A, V_{GS} = 0V$
		UFN822 UFN823	–	–	1.5	V	$T_C = 25°C, I_S = 2.0A, V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	–	600	–	ns	$T_J = 150°C, I_F = 2.5A, dI_F/dt = 100 A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	–	3.5	–	μC	$T_J = 150°C, I_F = 2.5A, dI_F/dt = 100 A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

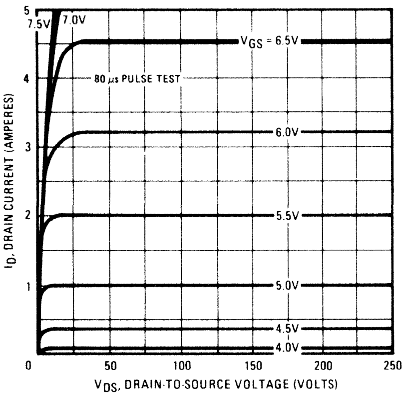


Fig. 2 — Typical Transfer Characteristics

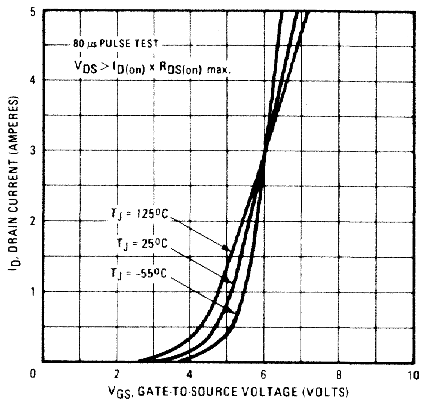


Fig. 3 — Typical Saturation Characteristics

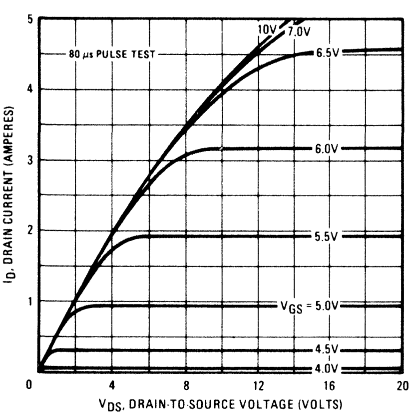


Fig. 4 — Maximum Safe Operating Area

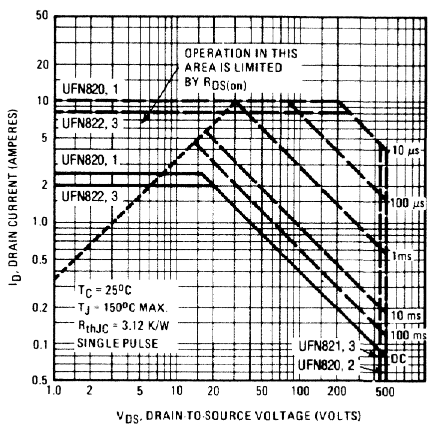


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Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

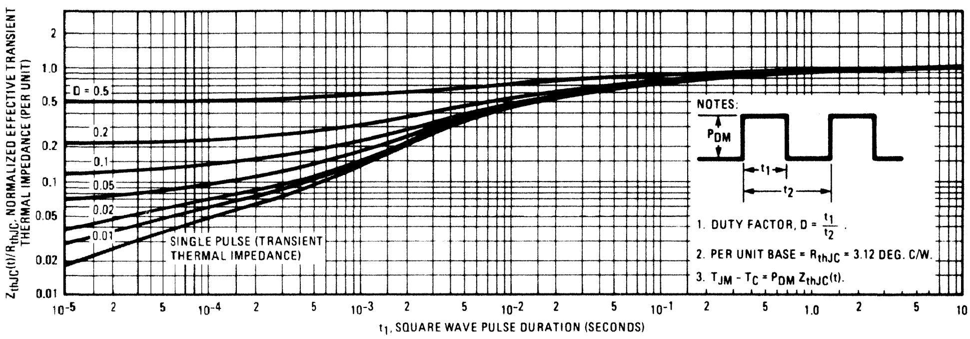


Fig. 6 — Typical Transconductance Vs. Drain Current

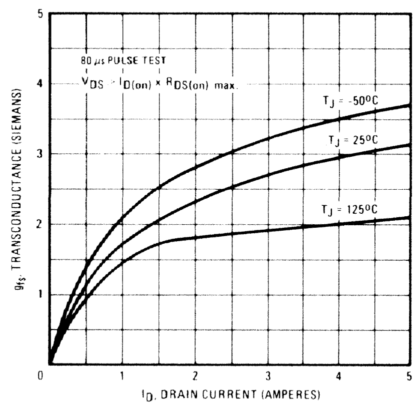


Fig. 7 — Typical Source-Drain Diode Forward Voltage

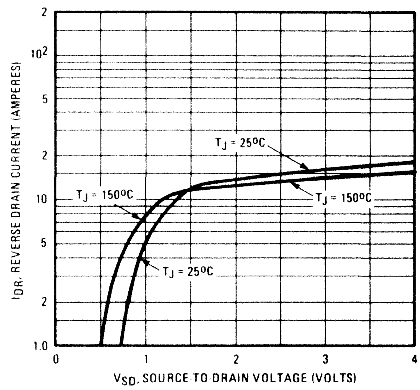


Fig. 8 — Breakdown Voltage Vs. Temperature

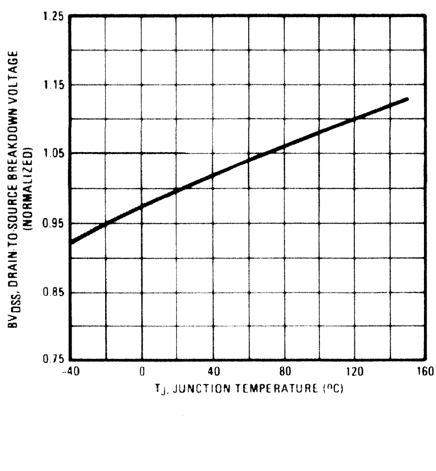


Fig. 9 — Normalized On-Resistance Vs. Temperature

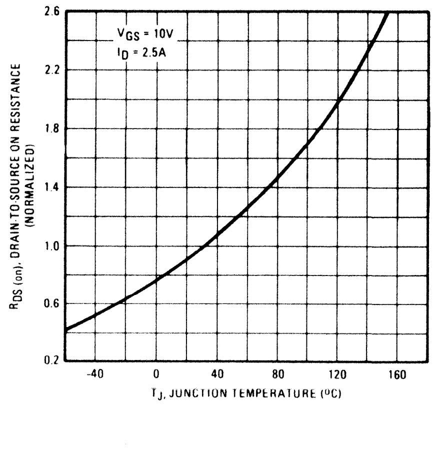


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

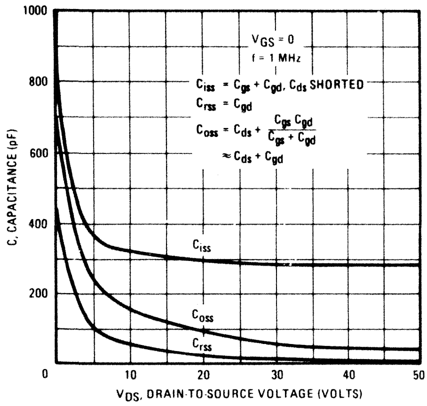


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

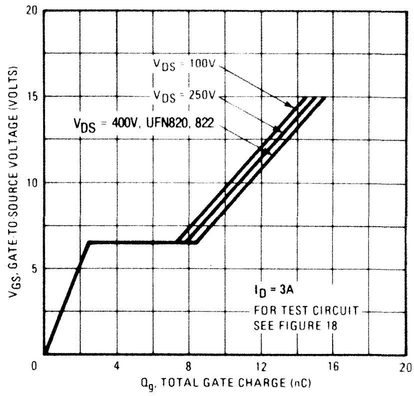


Fig. 12 — Typical On-Resistance Vs. Drain Current

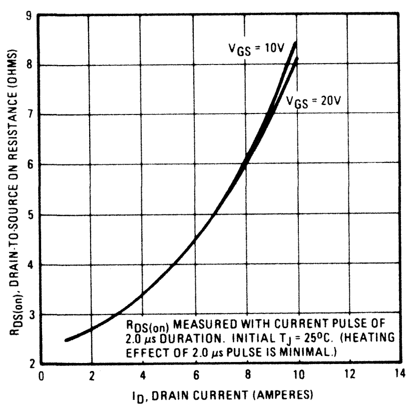


Fig. 13 — Maximum Drain Current Vs. Case Temperature

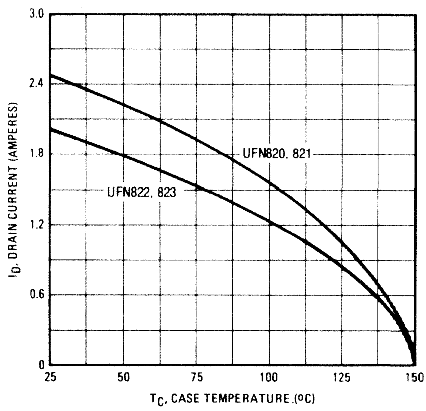


Fig. 14 — Power Vs. Temperature Derating Curve

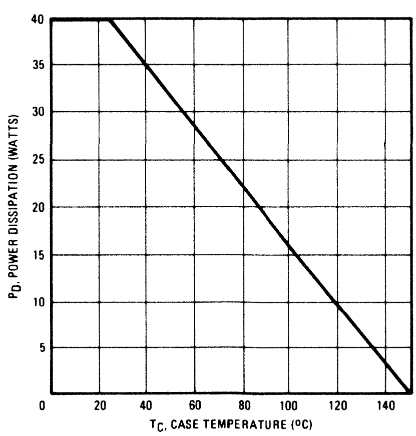


Fig. 15 — Clamped Inductive Test Circuit

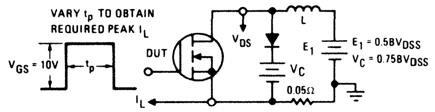


Fig. 16 — Clamped Inductive Waveforms

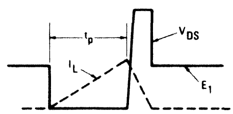


Fig. 17 — Switching Time Test Circuit

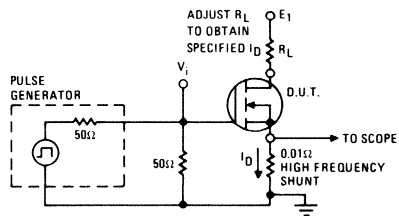
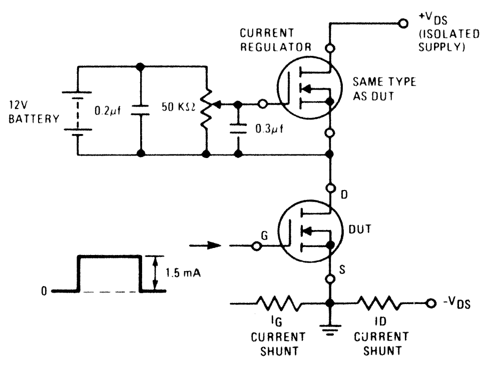


Fig. 18 — Gate Charge Test Circuit



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POWER MOSFET TRANSISTORS
500 Volt, 1.5 Ohm
N-Channel

UFN830
UFN831
UFN832
UFN833

FEATURES
- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION
The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

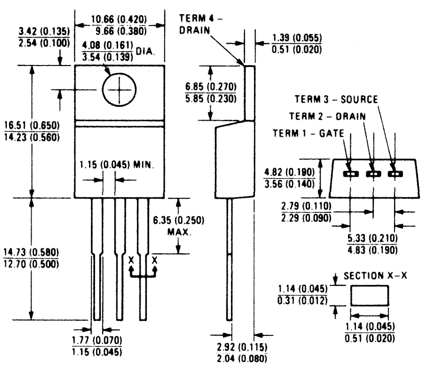
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN830	500V	1.5Ω	4.5A
UFN831	450V	1.5Ω	4.5A
UFN832	500V	2.0Ω	4.0A
UFN833	450V	2.0Ω	4.0A

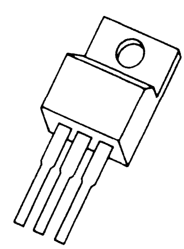
MECHANICAL SPECIFICATIONS

UFN830 UFN831 UFN832 UFN833



Dimensions in Millimeters and (Inches)

TO-220AB



UNITRODE

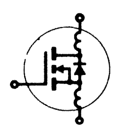
ABSOLUTE MAXIMUM RATINGS

Parameter		UFN830	UFN831	UFN832	UFN833	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	4.5	4.5	4.0	4.0	A
I_D @ T_C = 100°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_{DM}	Pulsed Drain Current ③	18	18	16	16	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 18	18	16	16	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFN830 UFN832	500	–	–	V	V_{GS} = 0V
		UFN831 UFN833	450	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFN830 UFN831	4.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)\,max.}$, V_{GS} = 10V
		UFN832 UFN833	4.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFN830 UFN831	–	1.3	1.5	Ω	V_{GS} = 10V, I_D = 2.5A
		UFN832 UFN833	–	1.5	2.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	2.5	3.25	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)\,max.}$, I_D = 2.5A
C_{iss}	Input Capacitance	ALL	–	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	100	200	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	30	60	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} ≈ 225V, I_D = 2.5A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	30	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	55	ns	
t_f	Fall Time	ALL	–	–	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	22	30	nC	V_{GS} = 10V, I_D = 6.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	11	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	11	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

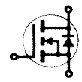
Modified MOSFET symbol showing the internal device inductances.



THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	K/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN830 UFN831	–	–	4.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFN832 UFN833	–	–	4.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN830 UFN831	–	–	18	A	
		UFN832 UFN833	–	–	16	A	
V_{SD}	Diode Forward Voltage ②	UFN830 UFN831	–	–	1.6	V	T_C = 25°C, I_S = 4.5A, V_{GS} = 0V
		UFN832 UFN833	–	–	1.5	V	T_C = 25°C, I_S = 4.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	800	–	ns	T_J = 150°C, I_F = 4.5A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.6	–	μC	T_J = 150°C, I_F = 4.5A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

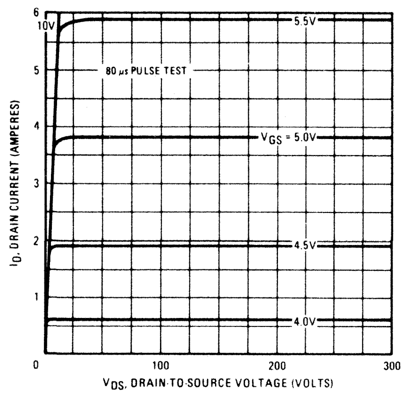


Fig. 2 — Typical Transfer Characteristics

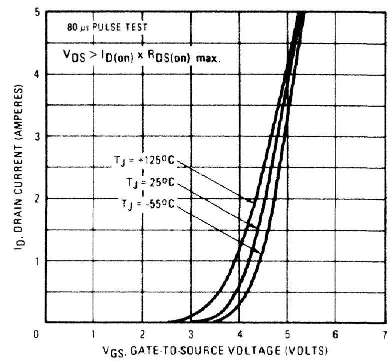


Fig. 3 — Typical Saturation Characteristics

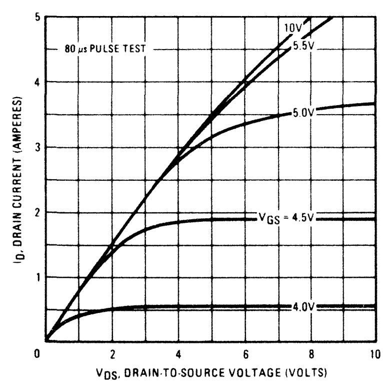


Fig. 4 — Maximum Safe Operating Area

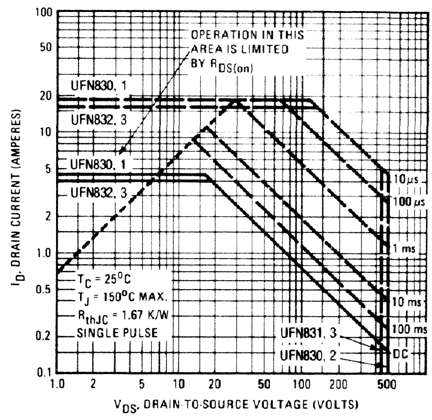


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

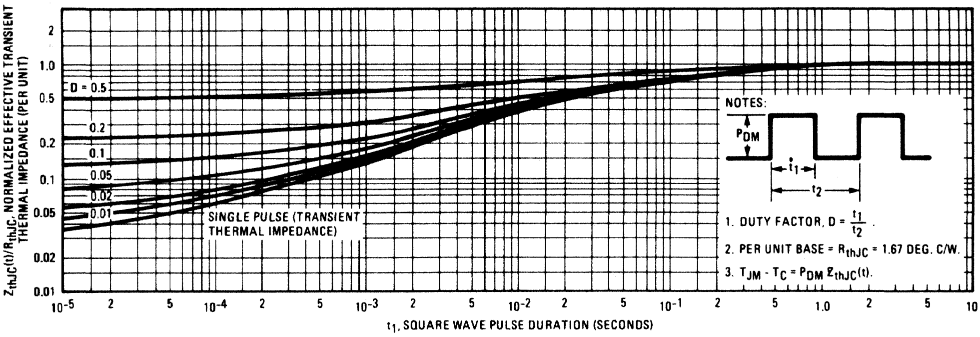


Fig. 6 — Typical Transconductance Vs. Drain Current

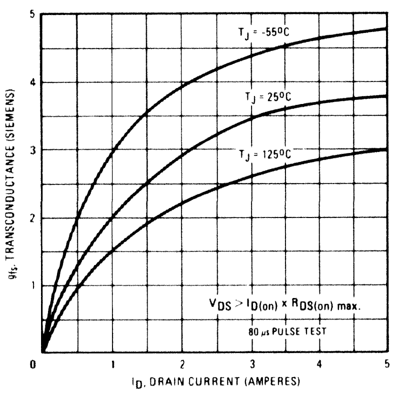


Fig. 7 — Typical Source-Drain Diode Forward Voltage

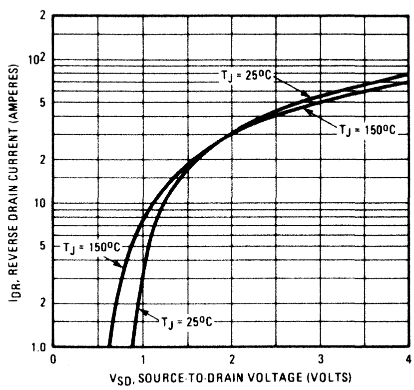


Fig. 8 — Breakdown Voltage Vs. Temperature

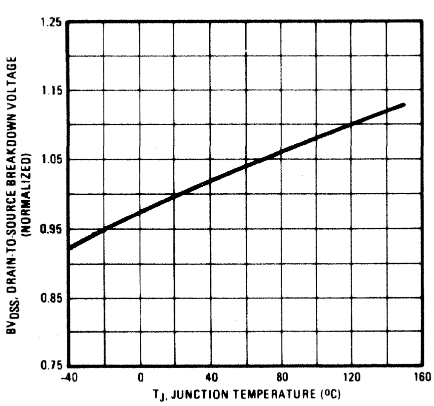


Fig. 9 — Normalized On-Resistance Vs. Temperature

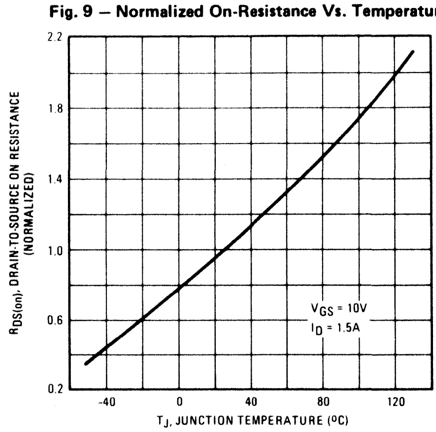


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

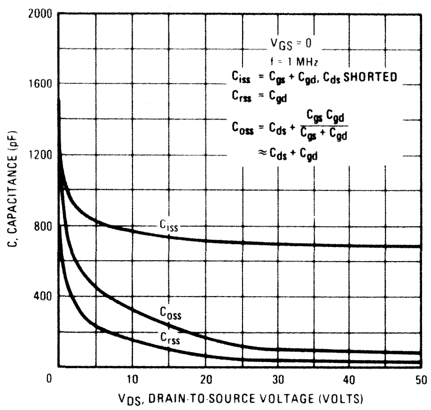


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

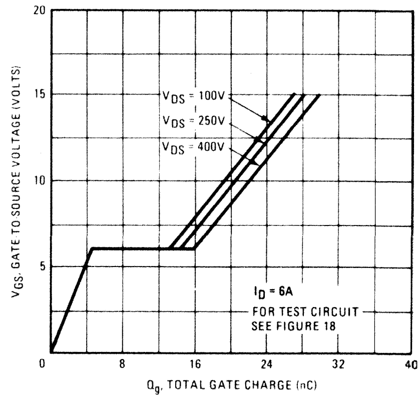


Fig. 12 – Typical On-Resistance Vs. Drain Current

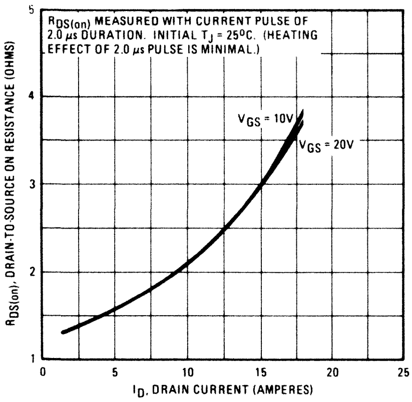


Fig. 13 – Maximum Drain Current Vs. Case Temperature

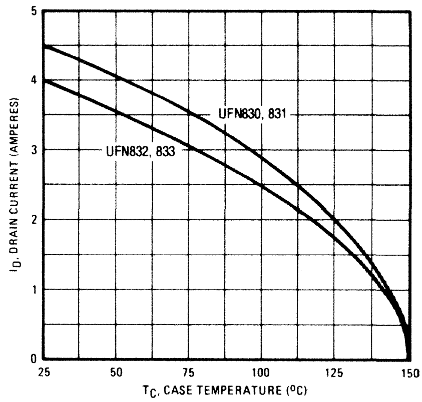


Fig. 14 – Power Vs. Temperature Derating Curve

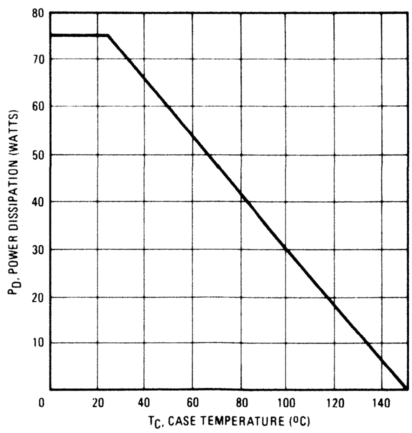


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Fig. 15 — Clamped Inductive Test Circuit

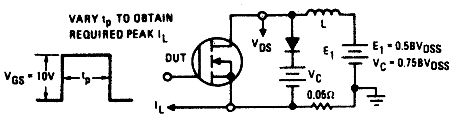


Fig. 16 — Clamped Inductive Waveforms

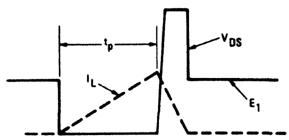


Fig. 17 — Switching Time Test Circuit

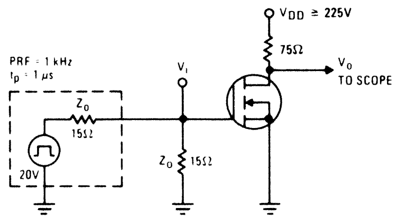
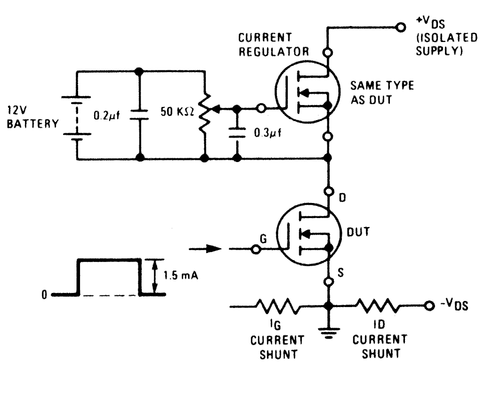


Fig. 18 — Gate Charge Test Circuit



POWER MOSFET TRANSISTORS
500 Volt, 0.85 Ohm
N-Channel

UFN840
UFN841
UFN842
UFN843

FEATURES
- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

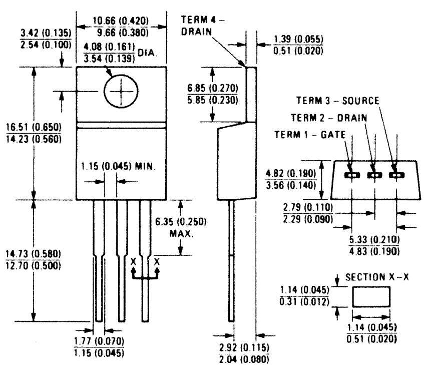
These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN840	500V	0.85Ω	8.0A
UFN841	450V	0.85Ω	8.0A
UFN842	500V	1.10Ω	7.0A
UFN843	450V	1.10Ω	7.0A

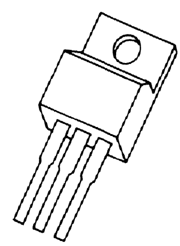
MECHANICAL SPECIFICATIONS

UFN840 UFN841 UFN842 UFN843



Dimensions in Millimeters and (Inches)

TO-220AB

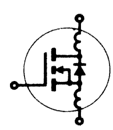


UNITRODE

ABSOLUTE MAXIMUM RATINGS

Parameter		UFN840	UFN841	UFN842	UFN843	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_D @ T_C = 100°C	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_{DM}	Pulsed Drain Current ③	32	32	28	28	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100µH 32	32	28	28	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions	
BV_{DSS}	Drain - Source Breakdown Voltage	UFN840 UFN842	500	–	–	V	V_{GS} = 0V	
		UFN841 UFN843	450	–	–	V	I_D = 250µA	
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250µA	
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V	
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V	
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	µA	V_{DS} = Max. Rating, V_{GS} = 0V	
			–	–	1000	µA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C	
$I_{D(on)}$	On-State Drain Current ②	UFN840 UFN841	8.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V	
		UFN842 UFN843	7.0	–	–	A		
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFN840 UFN841	–	0.1	1.0	Ω	V_{GS} = 10V, I_D = 4.0A	
		UFN842 UFN843	–	0.2	4.0	Ω		
g_{fs}	Forward Transconductance ②	ALL	4.0	6.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 4.0A	
C_{iss}	Input Capacitance	ALL	–	1225	1600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10	
C_{oss}	Output Capacitance	ALL	–	200	350	pF		
C_{rss}	Reverse Transfer Capacitance	ALL	–	85	150	pF		
$t_{d(on)}$	Turn-On Delay Time	ALL	–	17	35	ns	V_{DD} = 200V, I_D = 4.0A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t_r	Rise Time	ALL	–	5	15	ns		
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	42	90	ns		
t_f	Fall Time	ALL	–	14	30	ns		
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	42	60	nC	V_{GS} = 10V, I_D = 10A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q_{gs}	Gate-Source Charge	ALL	–	20	–	nC		
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	22	–	nC		
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.	Modified MOSFET symbol showing the internal device inductances. 
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.	
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.	

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	1.0	K/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

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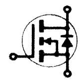
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN840 UFN841	–	–	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFN842 UFN843	–	–	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN840 UFN841	–	–	32	A	
		UFN842 UFN843	–	–	28	A	
V_{SD}	Diode Forward Voltage ②	UFN840 UFN841	–	–	2.0	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 100A/µs
		UFN842 UFN843	–	–	1.9	V	T_C = 25°C, I_S = 7.0A, V_{GS} = 100A/µs
t_{rr}	Reverse Recovery Time	ALL	–	1100	–	ns	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100 A/µs
Q_{RR}	Reverse Recovered Charge	ALL	–	6.4	–	µC	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100 A/µs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 — Typical Output Characteristics

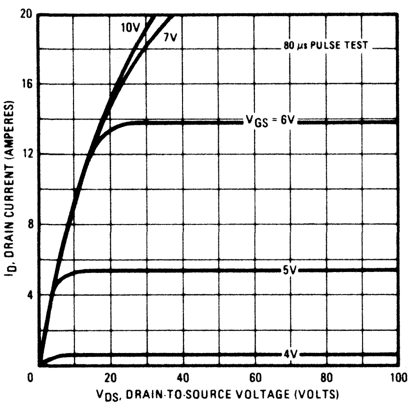


Fig. 2 — Typical Transfer Characteristics

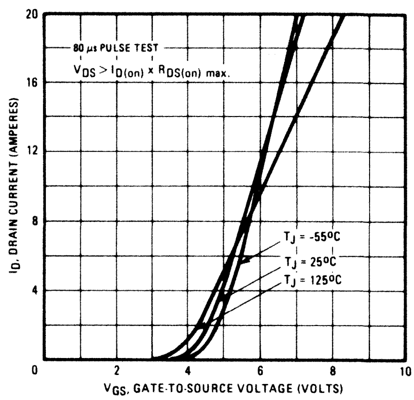


Fig. 3 — Typical Saturation Characteristics

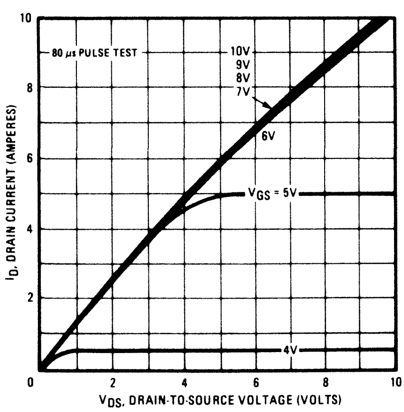


Fig. 4 — Maximum Safe Operating Area

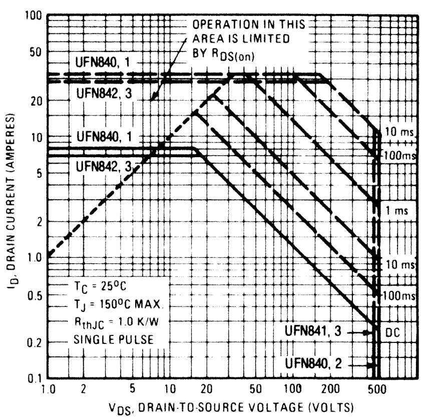


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

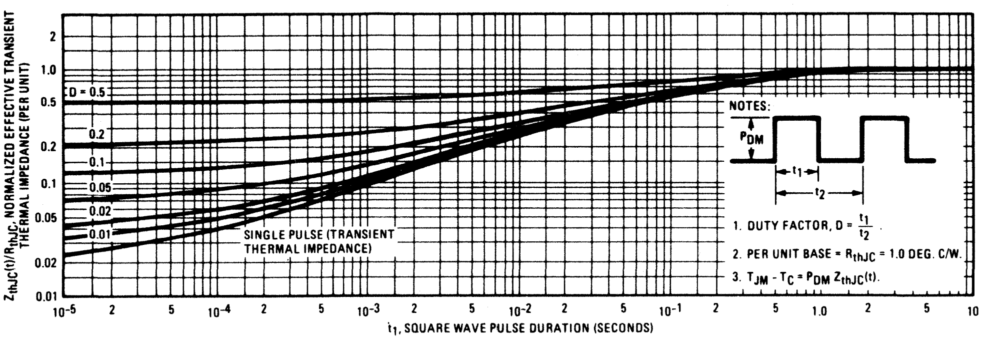


Fig. 6 — Typical Transconductance Vs. Drain Current

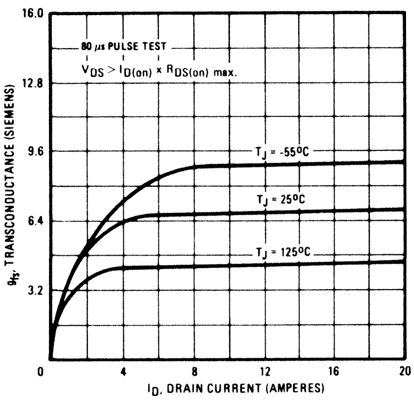


Fig. 7 — Typical Source-Drain Diode Forward Voltage

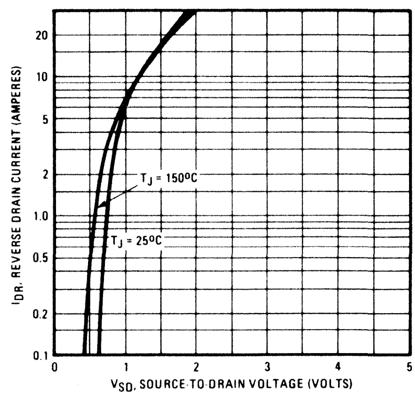


Fig. 8 — Breakdown Voltage Vs. Temperature

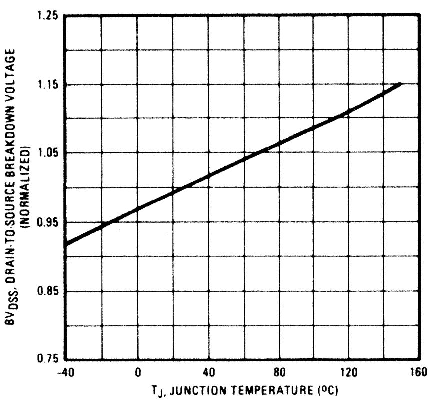


Fig. 9 — Normalized On-Resistance Vs. Temperature

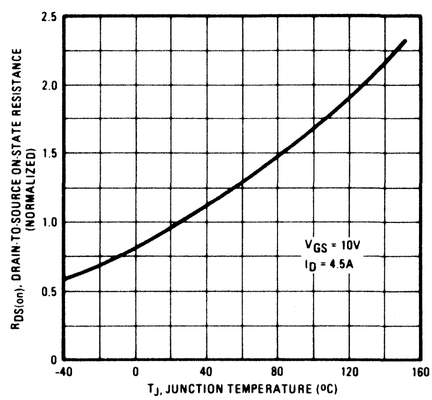


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

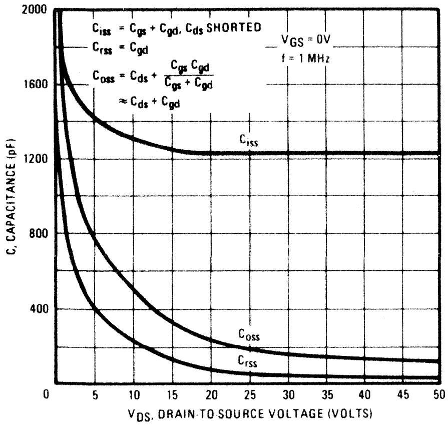


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

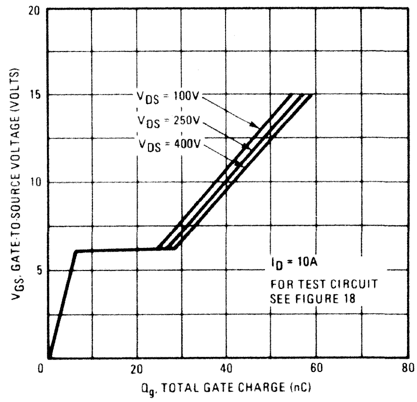


Fig. 12 — Typical On-Resistance Vs. Drain Current

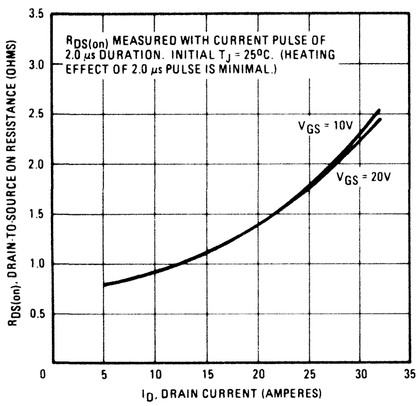


Fig. 13 — Maximum Drain Current Vs. Case Temperature

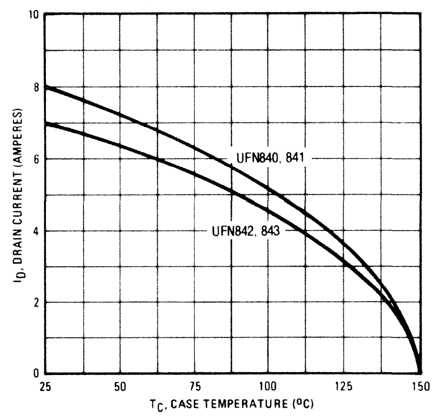


Fig. 14 — Power Vs. Temperature Derating Curve

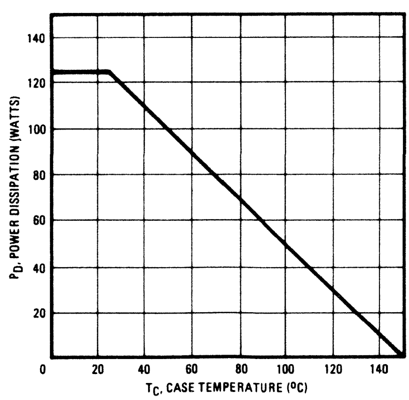


Fig. 15 — Clamped Inductive Test Circuit

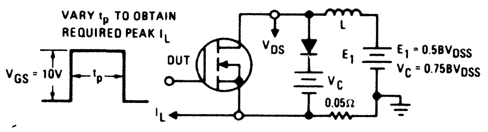


Fig. 16 — Clamped Inductive Waveforms

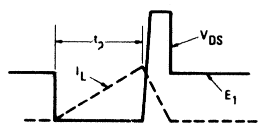


Fig. 17 — Switching Time Test Circuit

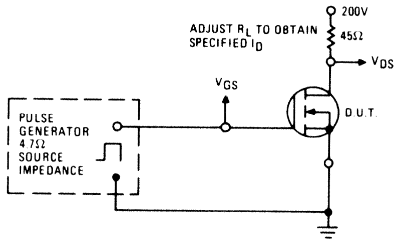
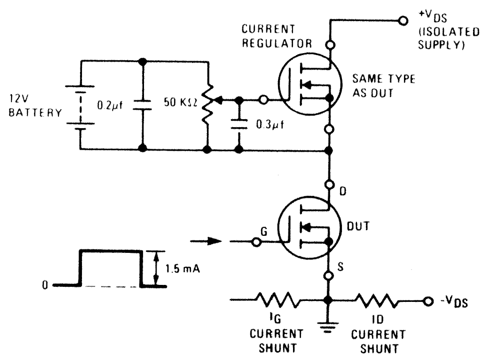


Fig. 18 — Gate Charge Test Circuit



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